TDA8954

2 × 210 W class-D power amplifier

Rev. 01 — 24 December 2009 | Product data sheet

1. General description

The TDA8954 is a stereo or mono high-efficiency Class D audio power amplifier in a single IC featuring low power dissipation. It is designed to deliver up to 2 × 210 W into a 4 Ω load in a stereo Single-Ended (SE) application, or 1 × 420 W into an 8 Ω load in a mono Bridge-Tied Load (BTL) application.

It combines the benefits of Class D efficiency (≈93 % into a 4 Ω load) with audiophile sound quality comparable to that associated with Class AB amplification.

The amplifier operates over a wide supply voltage range from ±12.5 V to ±42.5 V and features low quiescent current consumption.

The TDA8954 is supplied with two diagnostic pins for monitoring the status of Thermal Fold Back (TFB), Over Current Protection (OCP) and other protection circuits.

2. Features

- High output power in typical applications:
  - SE 2 × 210 W, R_L = 4 Ω (V_{DD} = 41 V; V_{SS} = –41 V)
  - SE 2 × 235 W, R_L = 3 Ω (V_{DD} = 39 V; V_{SS} = –39 V)
  - SE 2 × 150 W, R_L = 6 Ω (V_{DD} = 41 V; V_{SS} = –41 V)
  - BTL 1 × 420 W, R_L = 8 Ω (V_{DD} = 41 V; V_{SS} = –41 V)
- Symmetrical operating supply voltage range from ±12.5 V to ±42.5 V
- Stereo full differential inputs, can be used as stereo SE or mono BTL amplifier
- Low noise
- Smooth pop noise-free start-up and switch off
- 2-pin diagnostics for protection circuits
- Fixed frequency internal or external clock
- High efficiency ≈93 %
- Zero dead time switching
- Low quiescent current
- Advanced protection strategy: voltage protection and output current limiting
- Thermal FoldBack (TFB) with disable functionality
- Fixed gain of 30 dB in SE and 36 dB in BTL applications
- Fully short-circuit proof across load
- BD modulation in BTL configuration
- Clock protection

founded by Philips

3. Applications

- DVD
- Mini and micro receiver
- Subwoofers
- Home Theater In A Box (HTIAB) system
- High-power speaker system
- Public Address (PA) system

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
General							
V_{DD}	positive supply voltage	Operating mode	[1]	12.5	41	42.5	V
V_{SS}	negative supply voltage	Operating mode	[2]	–12.5	–41	–42.5	V
$V_{th(ovp)}$	overvoltage protection threshold voltage	Standby, Mute modes; $V_{DD} - V_{SS}$		85	-	90	V
$I_{DD(tot)}$	total positive supply current	the sum of the currents through pins VDDA, VDDP1 and VDDP2 Operating mode; no load; no filter; no RC-snubber network connected;		-	50	60	mA
$I_{SS(tot)}$	total negative supply current	the sum of the currents through pins VSSA, VSSP1 and VSSP2 Operating mode; no load; no filter; no RC-snubber network connected;		-	65	75	mA
Stereo single-ended configuration							
P_o	output power	T_j = 85 °C; L_{LC} = 15 μH; C_{LC} = 680 nF (see Figure 13)					
		THD + N = 10 %; R_L = 4 Ω; V_{DD} = 41 V; V_{SS} = –41 V	[3]	-	210	-	W
		THD + N = 10 %; R_L = 4 Ω; V_{DD} = 35 V; V_{SS} = –35 V		-	150	-	W
Mono bridge-tied load configuration							
P_o	output power	T_j = 85 °C; L_{LC} = 22 μH; C_{LC} = 680 nF (see Figure 13); R_L = 8 Ω; THD + N = 10 %; V_{DD} = 41 V; V_{SS} = –41 V	[3]	-	420	-	W

[1] V_{DD} is the supply voltage on pins VDDP1, VDDP2 and VDDA.

[2] V_{SS} is the supply voltage on pins VSSP1, VSSP2 and VSSA.

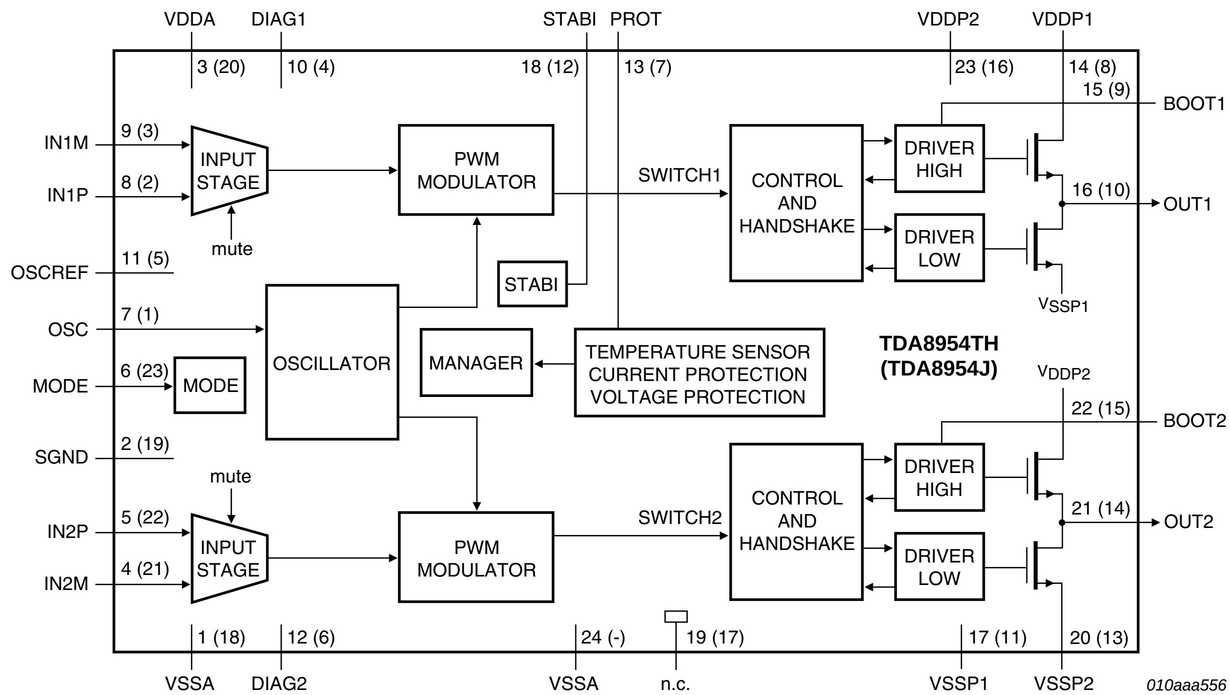
[3] Output power is measured indirectly; based on R_{DSon} measurement; see Section 14.3.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8954J	DBS23P	plastic DIL-bent-SIL power package; 23 leads (straight lead length 3.2 mm)	SOT411-1
TDA8954TH	HSOP24	plastic, heatsink small outline package; 24 leads; low stand-off height	SOT566-3

6. Block diagram



Pin numbers in brackets refer to type number TDA8954J.

Fig 1. Block diagram

7. Pinning information

7.1 Pinning

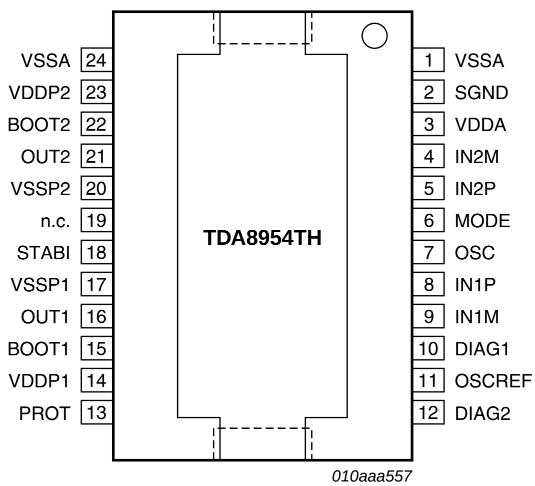


Fig 2. Pin configuration TDA8954TH

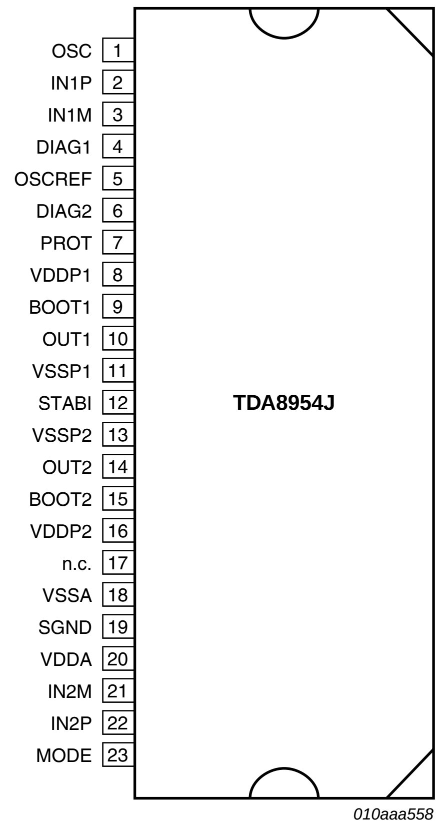


Fig 3. Pin configuration TDA8954J

7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TDA8954TH	TDA8954J	
VSSA	1	18	negative analog supply voltage
SGND	2	19	signal ground
VDDA	3	20	positive analog supply voltage
IN2M	4	21	channel 2 negative audio input
IN2P	5	22	channel 2 positive audio input
MODE	6	23	mode selection input: Standby, Mute or Operating mode
OSC	7	1	oscillator frequency adjustment or tracking input
IN1P	8	2	channel 1 positive audio input
IN1M	9	3	channel 1 negative audio input
DIAG1	10	4	diagnostic output 1 (open drain; TFB)
OSCREF	11	5	reference for OSC pin
DIAG2	12	6	diagnostic output 2 (open drain; protection functions)
PROT	13	7	decoupling capacitor for protection (OCP)
VDDP1	14	8	channel 1 positive power supply voltage
BOOT1	15	9	channel 1 bootstrap capacitor
OUT1	16	10	channel 1 PWM output
VSSP1	17	11	channel 1 negative power supply voltage
STABI	18	12	decoupling of internal stabilizer for logic supply
n.c.	19	17	not connected
VSSP2	20	13	channel 2 negative power supply voltage
OUT2	21	14	channel 2 PWM output
BOOT2	22	15	channel 2 bootstrap capacitor
VDDP2	23	16	channel 2 positive power supply voltage
VSSA	24	-	negative analog supply voltage

8. Functional description

8.1 General

The TDA8954 is a two-channel audio power amplifier that uses Class D technology.

For each channel, the audio input signal is converted into a digital Pulse Width Modulation (PWM) signal using an analog input stage and a PWM modulator; see Figure 1. To drive the output power transistors, the digital PWM signal is fed to a control and handshake block and to high- and low-side driver circuits. This level-shifts the low-power digital PWM signal from a logic level to a high-power PWM signal switching between the main supply lines.

A second-order low-pass filter converts the PWM signal to an analog audio signal that can be used to drive a loudspeaker.

The TDA8954 single-chip Class D amplifier contains high-power switches, drivers, timing and handshaking between the power switches, along with some control logic. To ensure maximum system robustness, an advanced protection strategy has been implemented to provide overvoltage, overtemperature and overcurrent protection.

Each of the two audio channels contains a PWM modulator, an analog feedback loop and a differential input stage. The TDA8954 also contains circuits common to both channels such as the oscillator, all reference sources, the mode interface and a digital timing manager.

The two independent amplifier channels feature high output power, high efficiency, low distortion and low quiescent currents. They can be connected in the following configurations:

- Stereo Single-Ended (SE)
- Mono Bridge-Tied Load (BTL)

The amplifier system can be switched to one of three operating modes using pin MODE:

- Standby mode: featuring very low quiescent current
- Mute mode: the amplifier is operational but the audio signal at the output is suppressed by disabling the voltage-to-current (VI) converter input stages
- Operating mode: the amplifier is fully operational, de-muted and can deliver an output signal

A slowly rising voltage should be applied (e.g. via an RC network) to pin MODE to ensure pop noise-free start-up. The bias-current setting of the (VI converter) input stages is related to the voltage on the MODE pin.

In Mute mode, the bias-current setting of the VI converters is zero (VI converters are disabled). In Operating mode, the bias current is at a maximum. The time constant required to apply the DC output offset voltage gradually between Mute and Operating mode levels can be generated using an RC network connected to pin MODE. An example of a circuit for driving the MODE pin, optimized for optimal pop noise performance, is shown in Figure 4. If the capacitor was omitted, the very short switching time constant could result in audible pop noises being generated at start-up (depending on the DC output offset voltage and loudspeaker used).

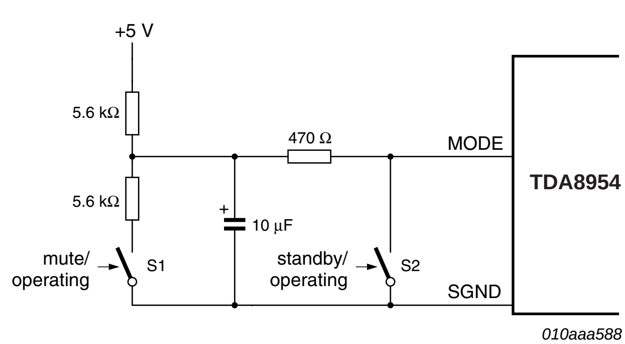
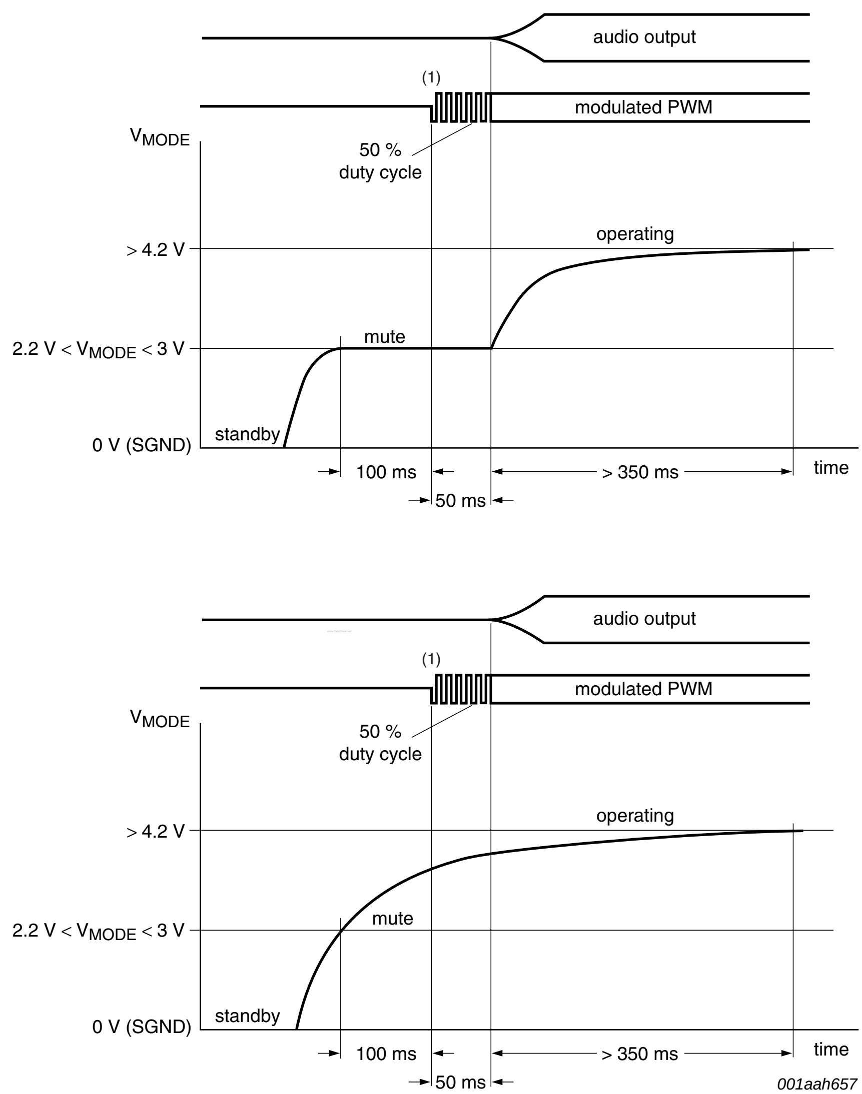


Fig 4. Example of mode selection circuit

The smooth transition between Mute and Operating modes causes a gradual increase in the DC offset output voltage, which becomes inaudible (no pop noise because the DC offset voltage rises smoothly). An overview of the start-up timing is provided in Figure 5. For proper switch-off, the MODE pin should be forced LOW at least 100 ms before the supply lines (V_{DD} and V_{SS}) drop below 12.5 V.



(1) First ¼ pulse down.

Upper diagram: When switching from Standby to Mute, there is a delay of approximately 100 ms before the output starts switching. The audio signal will become available once V_{MODE} reaches the Operating mode level (see Table 9), but not earlier than 150 ms after switching to Mute. To start-up pop noise-free, it is recommended that the time constant applied to pin MODE be at least 350 ms for the transition between Mute and Operating modes.

Lower diagram: When switching directly from Standby to Operating mode, there is a delay of 100 ms before the outputs start switching. The audio signal becomes available after a second delay of 50 ms. To start-up pop noise-free, it is recommended that the time-constant applied to pin MODE be at least 500 ms for the transition between Standby and Operating modes.

Fig 5. Timing on mode selection input pin MODE

8.2 Diagnostics

The TDA8954 provides two diagnostic signals on pins DIAG1 and DIAG2. Both are open-drain outputs that can be pulled up via a resistor (10 kΩ recommended) to a maximum of 5 V relative to the GND pin. The maximum input current on these pins is 1 mA.

Pin DIAG1 provides a TFB warning signal. Pin DIAG2 can be used to monitor the OCP status and the protection status (whether one of the protection circuits has switched off the amplifier).

Details of the timing of these signals can be found in Section 8.4.1.1 and Section 8.4.2; see also Table 5.

8.3 Pulse-width modulation frequency

The amplifier output signal is a PWM signal with a typical carrier frequency of between 250 kHz and 450 kHz. A second-order LC demodulation filter on the output converts the PWM signal into an analog audio signal. The carrier frequency, f_{OSC}, is determined by an external resistor, R_{OSC}, connected between pins OSC and OSCREF. The optimal carrier frequency setting is between 250 kHz and 450 kHz.

The carrier frequency is set to 335 kHz by connecting an external 30 kΩ resistor between pins OSC and OSCREF (see Figure 6).

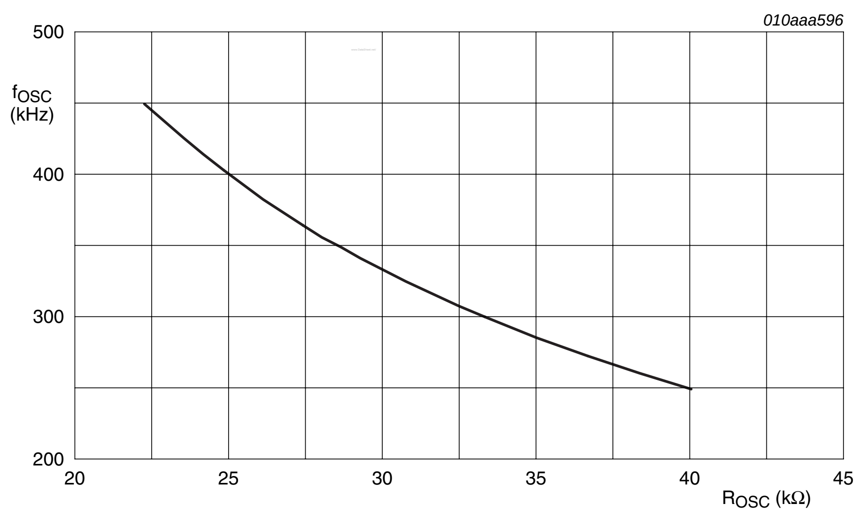


Fig 6. Carrier frequency as a function of R_{OSC}

If two or more Class D amplifiers are used in the same audio application, an external clock circuit must be used to synchronize all amplifiers (see Section 14.4). This will ensure that they operate at the same switching frequency, thus avoiding beat tones (if the switching frequencies are different, audible interference known as ‘beat tones’ can be generated).

8.4 Protection

The following protection circuits are incorporated into the TDA8954:

- Thermal protection:
  - Thermal FoldBack (TFB)
  - OverTemperature Protection (OTP)
- OverCurrent Protection (OCP)
- Window Protection (WP)
- Supply voltage protection:
  - UnderVoltage Protection (UVP)
  - OverVoltage Protection (OVP)
  - UnBalance Protection (UBP)
- Clock Protection (CP)

How the device reacts to a fault condition depends on which protection circuit has been activated.

8.4.1 Thermal protection

The TDA8954 employs an advanced thermal protection strategy. A TFB function gradually reduces the output power within a defined temperature range. If the temperature continues to rise, OTP is activated to shut the device down completely.

8.4.1.1 Thermal FoldBack (TFB)

If the junction temperature (T_j) exceeds the thermal foldback activation threshold ($T_{act(th\_fold)}$), the gain is gradually reduced. This reduces the output signal amplitude and the power dissipation, eventually stabilizing the temperature.

When T_j reaches $T_{act(warn)th\_fold}$, the TFB warning signal is activated (pin DIAG1 goes LOW). Thermal foldback is activated if the temperature rises to $T_{act(th\_fold)}$ (see Figure 7).

The TFB warning signal is reset when the temperature drops below $T_{rst(warn)th\_fold}$ again (see Figure 8).

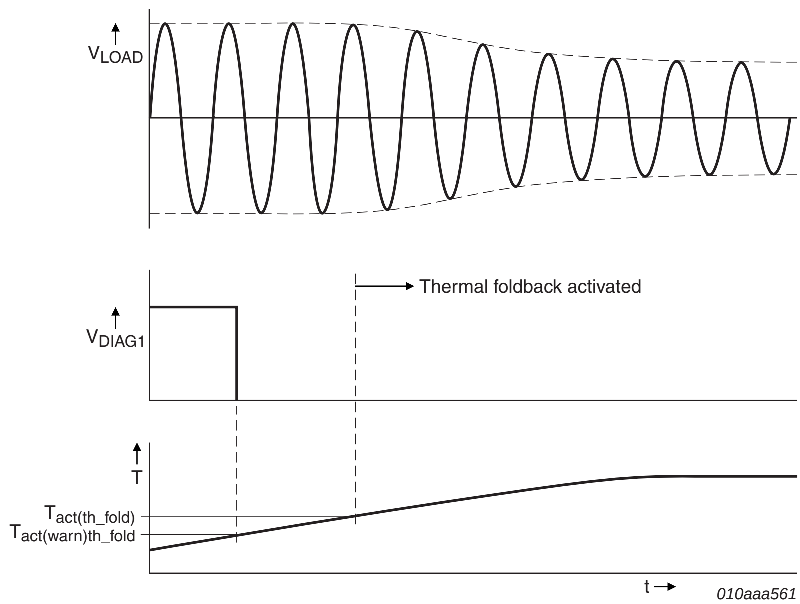


Fig 7. TFB and TFB warning

Thermal foldback is active when:

$T_{act(th\_fold)} < T_j < T_{act(th\_prot)}$

The value of $T_{act(th\_fold)}$ for the TDA8954 is approximately 145 °C; see Table 9 for more details. The gain will be reduced by at least 6 dB (to $T_{hg(th\_fold)}$) before the temperature reaches $T_{act(th\_prot)}$ (see Figure 8).

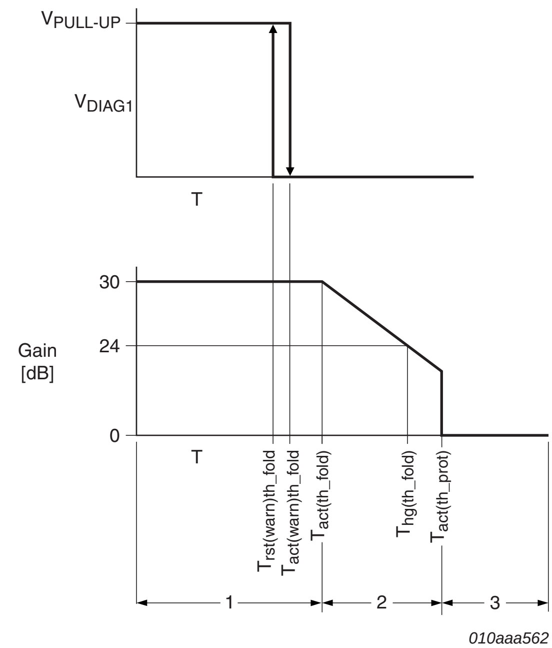
TFB can be disabled by applying the appropriate voltage on pin MODE (see Table 9), in which case the dissipation will not be limited by TFB. The junction temperature may then rise as high as the OTP threshold, when the amplifier will be shut down (see Section 8.4.1.2). The amplifier will start up again once it has cooled down. This introduces audio holes.

The TFB warning signal is not disabled when the TFB is disabled via the MODE pin. This allows a temperature control function in the application to monitor the junction temperature and, if necessary, to reduce the level of the audio signal transmitted to the amplifier.

8.4.1.2 OverTemperature Protection (OTP)

If TFB fails to stabilize the temperature and the junction temperature continues to rise, the amplifier will shut down as soon as the temperature reaches the thermal protection activation threshold, $T_{act(th\_prot)}$. The amplifier will resume switching approximately 100 ms after the temperature drops below $T_{act(th\_prot)}$.

The thermal behavior is illustrated in Figure 8.



(1) Duty cycle of PWM output modulated according to the audio input signal.

(2) Duty cycle of PWM output reduced due to TFB.

(3) Amplifier is switched off due to OTP.

Fig 8. Behavior of TFB, OTP and signal on pin DIAG1

8.4.2 OverCurrent Protection (OCP)

In order to guarantee the robustness of the TDA8954, the maximum output current delivered at the output stages is limited. OCP is built in for each output power switch.

OCP is activated when the current in one of the power transistors exceeds the OCP threshold (I_{ORM} = 12 A) due, for example, to a short-circuit to a supply line or across the load.

The TDA8954 amplifier distinguishes between low-ohmic short-circuit conditions and other overcurrent conditions such as a dynamic impedance drop at the loudspeaker. The impedance threshold (Z_{th}) depends on the supply voltage.

How the amplifier reacts to a short circuit depends on the short-circuit impedance:

- Short-circuit impedance > Z_{th}: the amplifier limits the maximum output current to I_{ORM} but the amplifier does not shut down the PWM outputs. Effectively, this results in a clipped output signal across the load (behavior very similar to voltage clipping).
- Short-circuit impedance < Z_{th}: the amplifier limits the maximum output current to I_{ORM} and at the same time discharges the capacitor on pin PROT. When C_{PROT} is fully discharged, the amplifier shuts down completely and an internal timer is started.

The value of the protection capacitor (C_{PROT}) connected to pin PROT can be between 10 pF and 220 pF (typically 47 pF). While OCP is activated, an internal current source is enabled that will discharge C_{PROT}.

When OCP is activated, the active power transistor is turned off and the other power transistor is turned on to reduce the current (C_{PROT} is partially discharged). Normal operation is resumed at the next switching cycle (C_{PROT} is recharged). C_{PROT} is partially discharge each time OCP is activated during a switching cycle. If the fault condition that caused OCP to be activated persists long enough to fully discharge C_{PROT}, the amplifier will switch off completely and a restart sequence will be initiated.

After a fixed period of 100 ms, the amplifier will attempt to switch on again, but will fail if the output current still exceeds the OCP threshold. The amplifier will continue trying to switch on every 100 ms. The average power dissipation will be low in this situation because the duty cycle is short.

Switching the amplifier on and off in this way will generate unwanted ‘audio holes’. This can be avoided by increasing the value of C_{PROT} (up to 220 pF) to delay amplifier switch-off. C_{PROT} will also prevent the amplifier switching off due to transient frequency-dependent impedance drops at the speakers.

The amplifier will switch on, and remain in Operating mode, once the overcurrent condition has been removed. OCP ensures the TDA8954 amplifier is fully protected against short-circuit conditions while avoiding audio holes.

Table 4. Current limiting behavior during low output impedance conditions at different values of C_{PROT}

Type	V_{DD}/V_{SS} (V)	V_I (mV, p-p)	f (Hz)	C_{PROT} (pF)	PWM output stops		
					Short (Z_{th} = 0 Ω)	Short (Z_{th} = 0.5 Ω)	Short (Z_{th} = 1 Ω)
TDA8954	+41/–41	500	20	10	yes[1]	yes[1]	yes[1]
			1000	10	yes	no	no
			20	15	yes[1]	yes[1]	yes[1]
			1000	15	yes	no	no
			1000	220	no	no	no

[1] OVP can be triggered by supply pumping; see Section 14.6.

Pin DIAG2 pin can be used to:

1. Monitor the OCP status - a pulsed signal at the switching frequency is generated on DIAG2 when current limiting has been enabled.
2. Monitor the protection status - a pulsed signal with a minimum width of typically 100 ms will be generated on pin DIAG2 to indicate that the amplifier has been switched off by one of the protection circuits (see Table 5). This signal is also generated at start-up before the amplifier output starts switching.

When a short circuit occurs between the load and the supply voltage, the current will increase rapidly to I_{ORM}, when current limiting will be activated. A pulsed signal at the switching frequency will be transmitted on pin DIAG2 to indicate that OCP is active. If the short circuit condition persists long enough to cause the OCP circuit to shut down the amplifier, the DIAG2 signal will be transmitted continuously until the amplifier has started up again and has commenced switching (see Figure 9).

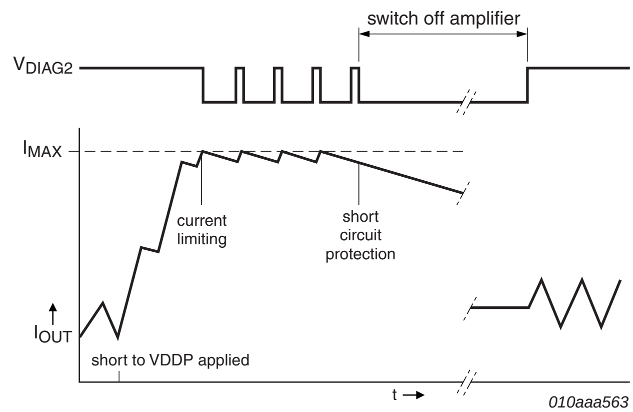


Fig 9. Current limiting

8.4.3 Window Protection (WP)

Window Protection (WP) checks the conditions at the output terminals of the power stage and is activated:

- During the start-up sequence, when the TDA8954 is switching from Standby to Mute.

  Start-up will be interrupted if a short-circuit is detected between one of the output terminals and one of the supply pins. The TDA8954 will wait until the short-circuit to the supply lines has been removed before resuming start-up. The short circuit will not generate large currents because the short-circuit check is carried out before the power stages are enabled.
- When the amplifier is shut down completely because the OCP circuit has detected a short circuit to one of the supply lines.

  WP will be activated when the amplifier attempts to restart after 100 ms (see Section 8.4.2). The amplifier will not start-up again until the short circuit to the supply lines has been removed.

8.4.4 Supply voltage protection

If the supply voltage drops below the minimum supply voltage threshold, $V_{th(uvp)}$, the UVP circuit will be activated and the system will shut down. Once the supply voltage rises above $V_{th(uvp)}$ again, the system will restart after a delay of 100 ms.

If the supply voltage exceeds the maximum supply voltage threshold, $V_{th(ovp)}$, the OVP circuit will be activated and the power stages will be shut down. When the supply voltage drops below $V_{th(ovp)}$ again, the system will restart after a delay of 100 ms.

An additional UnBalance Protection (UBP) circuit compares the positive analog supply voltage (on pin VDDA) with the negative analog supply voltage (on pin VSSA) and is triggered if the voltage difference exceeds a factor of two ($V_{DDA} > 2 \times |V_{SSA}|$ OR $|V_{SSA}| > 2 \times V_{DDA}$). When the supply voltage difference drops below the unbalance threshold, $V_{th(ubp)}$, the system restarts after 100 ms.

8.4.5 Clock protection (CP)

The clock signal can be provided by an external oscillator connected to pin OSC (see Section 14.4). When this signal is lost, or the clock frequency is too low, the amplifier will be switched off and will remain off until the clock signal has been restored.

8.4.6 Overview of protection functions

An overview of all protection circuits and their respective effects on the output signal is provided in Table 5.

Table 5. Overview of TDA8954 protection circuits

Protection name	Complete shutdown	Restart directly	Restart after 100 ms	PROT pin active	DIAG1 pin active	DIAG2 pin active
TFB[1]	N	N	N	N	Y[2]	N
OTP	Y	N	Y	N	N	Y
OCP	Y[3]	N[3]	Y[3]	Y	N	Y
WP	N[4]	Y	N	N	N	Y
UVP	Y	N	Y	N	N	Y
OVP	Y	N	Y	N	N	Y
UBP	Y	N	Y	N	N	Y
CP	Y	N	Y[5]	N	N	Y

[1] Amplifier gain depends on the junction temperature.

[2] TFB warning signal on pin DIAG1 is activated before TFB is enabled.

[3] The amplifier shuts down completely only if the short-circuit impedance is below the impedance threshold (Z_{th}; see Section 8.4.2). In all other cases, current limiting results in a clipped output signal.

[4] Fault condition detected during any Standby-to-Mute transition or during a restart after OCP has been activated (short-circuit to one of the supply lines).

[5] As soon as the clock is present.

8.5 Differential audio inputs

The audio inputs are fully differential ensuring a high common mode rejection ratio and maximum flexibility in the application.

- Stereo operation: to avoid supply pumping effects and to minimize peak currents in the power supply, the output stages should be configured in anti-phase. To avoid acoustical phase differences, the speakers should also be connected in anti-phase.
- Mono BTL operation: the inputs must be connected in anti-parallel. The output of one channel is inverted and the speaker load is connected between the two outputs of the TDA8954. In practice (because of the OCP threshold) the maximum output power in the BTL configuration can be boosted to twice the maximum output power available in the single-ended configuration.

  The input configuration for a mono BTL application is illustrated in Figure 10.

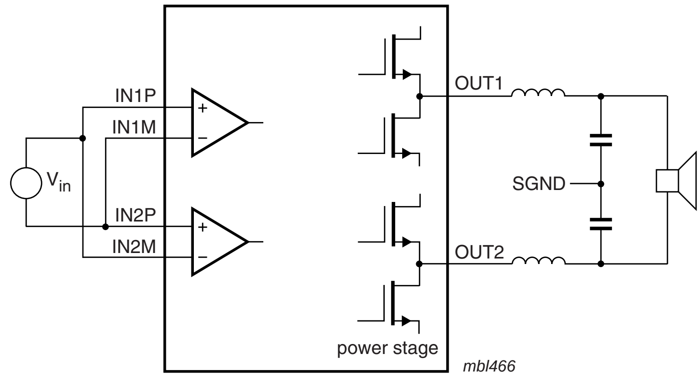


Fig 10. Input configuration for mono BTL application

9. Internal circuitry

Table 6. Internal circuitry

<table>
<tr><th colspan="2">Pin</th><th rowspan="2">Symbol</th><th rowspan="2">Equivalent circuit[1]</th></tr>
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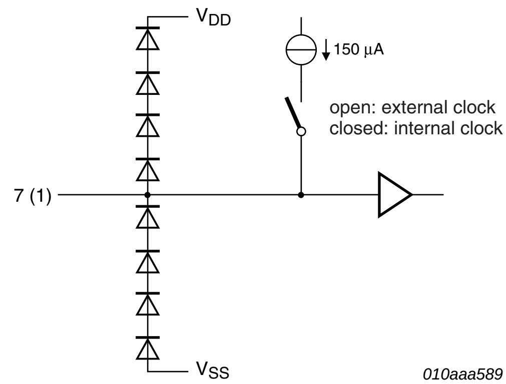
<tr><td>7</td><td>1</td><td>OSC</td><td>
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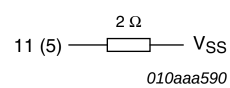
<tr><td>11</td><td>5</td><td>OSCREF</td><td>
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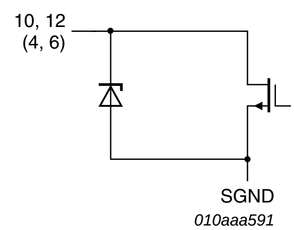
<tr><td>10</td><td>4</td><td>DIAG1</td><td rowspan="2">
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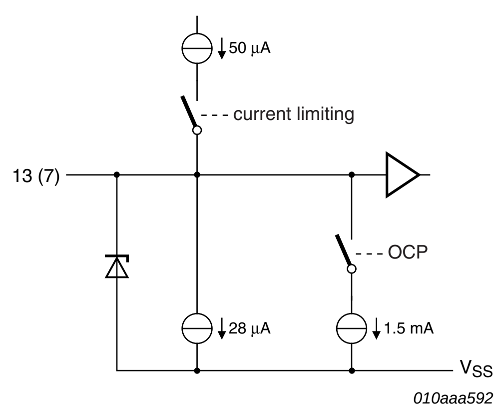
<tr><td>13</td><td>7</td><td>PROT</td><td>
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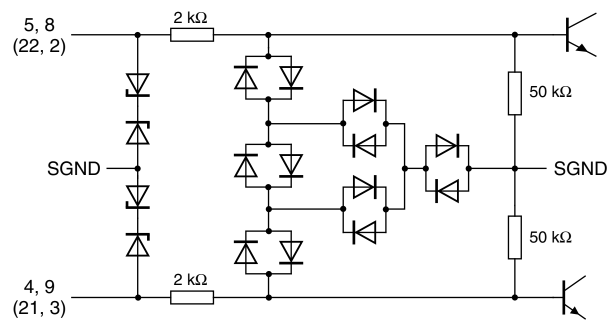
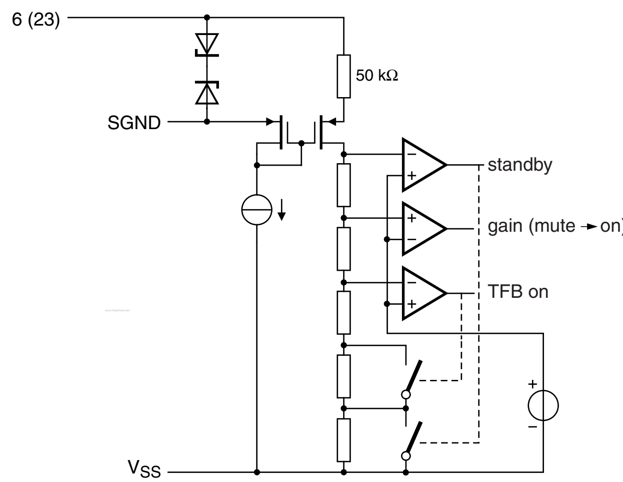
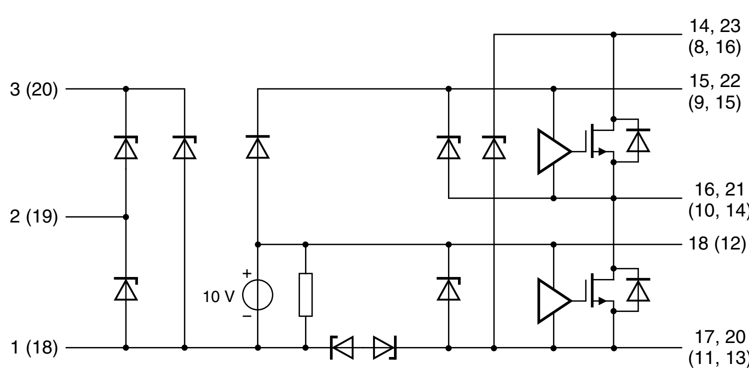
Table 6. Internal circuitry *…continued*

Pin		Symbol	Equivalent circuit[1]
TDA8954TH	TDA8954J		
4	21	IN2M	 010aaa593
5	22	IN2P	
8	2	IN1P	
9	3	IN1M	
6	23	MODE	 010aaa594
1	18	VSSA	 010aaa595
2	19	SGND	
3	20	VDDA	
14	8	VDDP1	
15	9	BOOT1	
16	10	OUT1	
17	11	VSSP1	
18	12	STABI	
20	13	VSSP2	
21	14	OUT2	
22	15	BOOT2	
23	16	VDDP2	

[1] Pin numbers in brackets are for the TDA8954J

10. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
ΔV	voltage difference	$V_{DD} - V_{SS}$; Standby, Mute modes	-	90	V
I_{ORM}	repetitive peak output current	maximum output current limiting; one channel driven	12	-	A
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		-	150	°C
V_{OSC}	voltage on pin OSC	relative to V_{SSA}	0	SGND + 6	V
V_{pu}	pull-up voltage	on pins DIAG1 and DIAG2; see Figure 13	0	5	V
V_I	input voltage	referenced to SGND; on pins IN1P, IN1M, IN2P and IN2M	–5	+5	V
V_{PROT}	voltage on pin PROT	referenced to voltage on pin VSSA	0	12	V
V_{MODE}	voltage on pin MODE	referenced to SGND	0	8	V
I_I	input current	on pins DIAG1 and DIAG2	0	1	mA
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM)	–2000	+2000	V
		Charged Device Model (CDM)	–500	+500	V
$V_{PWM(p-p)}$	peak-to-peak PWM voltage	on pins OUT1 and OUT2	-	120	V

11. Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		0.9	K/W

12. Static characteristics

Table 9. Static characteristics

V_{DD} = 41 V; V_{SS} = –41 V; f_{osc} = 335 kHz; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	positive supply voltage	Operating mode	[1]	12.5	41	42.5	V
V_{SS}	negative supply voltage	Operating mode	[2]	–12.5	–41	–42.5	V
$V_{th(ovp)}$	overvoltage protection threshold voltage	Standby, Mute modes; $V_{DD} - V_{SS}$		85	-	90	V
$V_{th(uvp)}$	undervoltage protection threshold voltage	$V_{DD} - V_{SS}$		20	-	25	V
$V_{th(ubp)}$	unbalance protection threshold voltage		[3]	-	33	-	%

Table 9. Static characteristics *...continued*

V_{DD} = 41 V; V_{SS} = −41 V; f_{osc} = 335 kHz; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DD(tot)}$	total positive supply current	the sum of the currents through pins VDDA, VDDP1 and VDDP2 Operating mode; no load; no filter; no RC-snubber network connected;		-	50	60	mA
$I_{SS(tot)}$	total negative supply current	the sum of the currents through pins VSSA, VSSP1 and VSSP2 Operating mode; no load; no filter; no RC-snubber network connected;		-	65	75	mA
I_{stb}	standby current			-	490	650	µA
Mode select input; pin MODE							
V_{MODE}	voltage on pin MODE	referenced to SGND	[4]	0	-	8	V
		Standby mode	[4][5]	0	-	0.8	V
		Mute mode	[4][5]	2.2	-	3.0	V
		Operating mode	[4][5]	4.2	-	5.5	V
		Operating mode without TFB	[4][5]	6.6	-	8	
I_I	input current	V_I = 5.5 V		-	110	150	µA
Audio inputs; pins IN1M, IN1P, IN2P and IN2M							
V_I	input voltage	DC input	[4]	-	0	-	V
Amplifier outputs; pins OUT1 and OUT2							
$V_{O(offset)}$	output offset voltage	SE; Mute mode		−37	-	+37	mV
		SE; Operating mode	[6]	−150	-	+150	mV
		BTL; Mute mode		−30	-	+30	mV
		BTL; Operating mode	[6]	−210	-	+210	mV
Stabilizer output; pin STABI							
$V_{O(STABI)}$	output voltage on pin STABI	Mute and Operating modes; with respect to VSSA		9.5	10	10.5	V
Temperature protection							
$T_{rst(warn)th\_fold}$	thermal foldback warning reset temperature			-	138	-	°C
$T_{act(warn)th\_fold}$	thermal foldback warning activation temperature			-	139	-	°C
$T_{act(th\_fold)}$	thermal foldback activation temperature	V_{MODE} < 5.5 V		-	145	-	°C
$T_{hg(th\_fold)}$	thermal foldback half gain temperature	V_{MODE} < 5.5 V; gain = 24 dB		-	153	-	°C
$T_{act(th\_prot)}$	thermal protection activation temperature			-	154	-	°C

[1] V_{DD} is the supply voltage on pins VDDP1, VDDP2 and VDDA.

[2] V_{SS} is the supply voltage on pins VSSP1, VSSP2 and VSSA.

[3] Unbalance protection activated when $V_{DDA} > 2 \times |V_{SSA}|$ OR $|V_{SSA}| > 2 \times V_{DDA}$.

[4] With respect to SGND (0 V).

[5] The transition between Standby and Mute modes has hysteresis, while the slope of the transition between Mute and Operating modes is determined by the time-constant of the RC network on pin MODE; see Figure 11.

[6] DC output offset voltage is gradually applied to the output during the transition between Mute and Operating modes. The slope caused by any DC output offset is determined by the time-constant of the RC network on pin MODE.

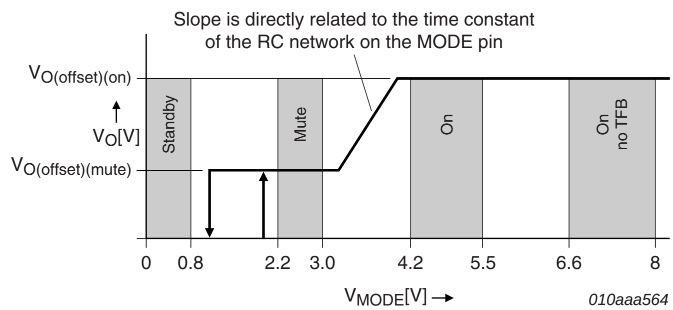


Fig 11. Behavior of mode selection pin MODE

13. Dynamic characteristics

13.1 Switching characteristics

Table 10. Dynamic characteristics

V_{DD} = 41 V; V_{SS} = −41 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Internal oscillator							
$f_{osc(typ)}$	typical oscillator frequency	R_{OSC} = 30.0 kΩ		290	335	365	kHz
f_{osc}	oscillator frequency			250	-	450	kHz
External oscillator input or frequency tracking; pin OSC							
V_{OSC}	voltage on pin OSC	HIGH-level		SGND + 4.5	SGND + 5	SGND + 6	V
V_{trip}	trip voltage			-	SGND + 2.5	-	V
f_{track}	tracking frequency		[1]	500	-	1000	kHz
Z_i	input impedance			1	-	-	MΩ
C_i	input capacitance			-	-	15	pF
$t_{r(i)}$	input rise time	from SGND + 0 V to SGND + 5 V	[2]	-	-	100	ns

[1] When using an external oscillator, the frequency f_{track} (500 kHz minimum, 1000 kHz maximum) will result in a PWM frequency f_{osc} (250 kHz minimum, 500 kHz maximum) due to the internal clock divider; see Section 8.3.

[2] When $t_{r(i)}$ > 100 ns, the output noise floor will increase.

13.2 Stereo SE configuration characteristics

Table 11. Dynamic characteristics

V_{DD} = 41 V; V_{SS} = −41 V; R_L = 4 Ω; f_i = 1 kHz; f_{osc} = 335 kHz; R_{sL} < 0.1 Ω[1]; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	L = 15 μH; C_{LC} = 680 nF; T_j = 85 °C	[2]				
		THD = 0.5 %; R_L = 4 Ω		-	160	-	W
		THD = 10 %; R_L = 4 Ω		-	210	-	W
		THD = 10 %; R_L = 3 Ω; V_P = ±39 V	[3]	-	235	-	W
THD	total harmonic distortion	P_o = 1 W; f_i = 1 kHz	[4]	-	0.03	0.1	%
		P_o = 1 W; f_i = 6 kHz	[4]	-	0.05	-	%
$G_{v(cl)}$	closed-loop voltage gain			29	30	31	dB
SVRR	supply voltage ripple rejection	between pins VDDPn and SGND					
		Operating mode; f_i = 100 Hz	[5]	-	90	-	dB
		Operating mode; f_i = 1 kHz	[5]	-	70	-	dB
		Mute mode; f_i = 100 Hz	[5]	-	75	-	dB
		Standby mode; f_i = 100 Hz	[5]	-	120	-	dB
		between pins VSSPn and SGND					
		Operating mode; f_i = 100 Hz	[5]	-	80	-	dB
		Operating mode; f_i = 1 kHz	[5]	-	60	-	dB
		Mute mode; f_i = 100 Hz	[5]	-	80	-	dB
		Standby mode; f_i = 100 Hz	[5]	-	115	-	dB
Z_i	input impedance	between an input pin and SGND		45	56	-	kΩ
$V_{n(o)}$	output noise voltage	Operating mode; inputs shorted	[6]	-	160	-	μV
		Mute mode	[7]	-	85	-	μV
α_{cs}	channel separation		[8]	-	70	-	dB
$\|\Delta G_v\|$	voltage gain difference			-	-	1	dB
α_{mute}	mute attenuation	f_i = 1 kHz; V_i = 2 V (RMS)	[9]	-	75	-	dB
CMRR	common mode rejection ratio	$V_{i(CM)}$ = 1 V (RMS)		-	75	-	dB
η_{po}	output power efficiency	SE, R_L = 4 Ω		-	93	-	%
		SE, R_L = 3 Ω		-	90	-	%
		BTL, R_L = 8 Ω		-	93	-	%
$R_{DSon(hs)}$	high-side drain-source on-state resistance		[10]	-	110	-	mΩ
$R_{DSon(ls)}$	low-side drain-source on-state resistance		[10]	-	105	-	mΩ

[1] R_{sL} is the series resistance of the low-pass LC filter inductor used in the application.

[2] Output power is measured indirectly; based on R_{DSon} measurement; see Section 14.3.

[3] One channel driven at maximum output power; the other channel driven at one eight maximum output power.

[4] THD measured between 22 Hz and 20 kHz, using AES17 20 kHz brick wall filter.

[5] V_{ripple} = $V_{ripple(max)}$ = 2 V (p-p); measured independently between VDDPn and SGND and between VSSPn and SGND.

[6] 22 Hz to 20 kHz, using AES17 20 kHz brick wall filter.

[7] 22 Hz to 20 kHz, using AES17 20 kHz brick wall filter.

[8] P_o = 1 W; f_i = 1 kHz.

[9] V_i = $V_{i(max)}$ = 1 V (RMS); f_i = 1 kHz.

[10] Leads and bond wires included.

13.3 Mono BTL application characteristics

Table 12. Dynamic characteristics

V_{DD} = 41 V; V_{SS} = −41 V; R_L = 8 Ω; f_i = 1 kHz; f_{osc} = 335 kHz; R_{sL} < 0.1 Ω [1]; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	T_j = 85 °C; L_{LC} = 15 μH; C_{LC} = 680 nF (see Figure 13)	[2]				
		THD = 0.5 %; R_L = 8 Ω		-	330	-	W
		THD = 10 %; R_L = 8 Ω		-	420	-	W
THD	total harmonic distortion	P_o = 1 W; f_i = 1 kHz	[3]	-	0.03	0.1	%
		P_o = 1 W; f_i = 6 kHz	[3]	-	0.05	-	%
$G_{v(cl)}$	closed-loop voltage gain			-	36	-	dB
SVRR	supply voltage ripple rejection	between pin VDDPn and SGND					
		Operating mode; f_i = 100 Hz	[5]	-	80	-	dB
		Operating mode; f_i = 1 kHz	[5]	-	80	-	dB
		Mute mode; f_i = 100 Hz	[5]	-	95	-	dB
		Standby mode; f_i = 100 Hz	[5]	-	120	-	dB
		between pin VSSPn and SGND					
		Operating mode; f_i = 100 Hz	[5]	-	75	-	dB
		Operating mode; f_i = 1 kHz	[5]	-	75	-	dB
		Mute mode; f_i = 100 Hz	[5]	-	90	-	dB
		Standby mode; f_i = 100 Hz	[5]	-	130	-	dB
Z_i	input impedance	measured between one of the input pins and SGND		45	56	-	kΩ
$V_{n(o)}$	output noise voltage	Operating mode; inputs shorted	[5]	-	190	-	μV
		Mute mode	[6]	-	45	-	μV
α_{mute}	mute attenuation	f_i = 1 kHz; V_i = 2 V (RMS)	[7]	-	75	-	dB
CMRR	common mode rejection ratio	$V_{i(CM)}$ = 1 V (RMS)		-	75	-	dB

[1] R_{sL} is the series resistance of the low-pass LC filter inductor used in the application.

[2] Output power is measured indirectly; based on R_{DSon} measurement; see Section 14.3.

[3] THD measured between 22 Hz and 20 kHz, using AES17 20 kHz brick wall filter.

[4] V_{ripple} = $V_{ripple(max)}$ = 2 V (p-p).

[5] 22 Hz to 20 kHz, using an AES17 20 kHz brick wall filter; low noise due to BD modulation.

[6] 22 Hz to 20 kHz, using an AES17 20 kHz brick wall filter.

[7] V_i = $V_{i(max)}$ = 1 V (RMS); f_i = 1 kHz.

14. Application information

14.1 Mono BTL application

When using the power amplifier in a mono BTL application, the inputs of the two channels must be connected in anti-parallel and the phase of one of the inputs must be inverted; see Figure 10. In principle, the loudspeaker can be connected between the outputs of the two single-ended demodulation filters.

14.2 Pin MODE

To ensure a pop noise-free start-up, an RC time-constant must be applied to pin MODE. The bias-current setting of the VI converter input is directly related to the voltage on pin MODE. In turn the bias-current setting of the VI converters is directly related to the DC output offset voltage. A slow dV/dt on pin MODE results in a slow dV/dt for the DC output offset voltage, ensuring a pop noise-free transition between Mute and Operating modes. A time-constant of 500 ms is sufficient to guarantee pop noise-free start-up; see Figure 4, Figure 5 and Figure 11 for more information.

14.3 Estimating the output power

14.3.1 Single-Ended (SE)

Maximum output power:

$$P_{o(0.5\%)} = \frac{\left[\frac{R_L}{R_L + R_{DSon(hs)} + R_{s(L)}} \times 0.5(V_{DD} - V_{SS}) \times (1 - t_{w(min)} \times 0.5 f_{osc})\right]^2}{2R_L} \qquad (1)$$

Maximum output current is internally limited to 12 A:

$$I_{o(peak)} = \frac{0.5(V_{DD} - V_{SS}) \times (1 - t_{w(min)} \times 0.5 f_{osc})}{R_L + R_{DSon(hs)} + R_{s(L)}} \qquad (2)$$

Where:

- $P_{o(0.5\,\%)}$: output power at the onset of clipping
- R_L: load impedance
- $R_{DSon(hs)}$: high-side R_{DSon} of power stage output DMOS (temperature dependent)
- $R_{s(L)}$: series impedance of the filter coil
- $t_{w(min)}$: minimum pulse width (typical 150 ns; temperature dependent)
- f_{osc}: oscillator frequency

Remark: Note that $I_{o(peak)}$ should be less than 12 A (Section 8.4.2). $I_{o(peak)}$ is the sum of the current through the load and the ripple current. The value of the ripple current is dependent on the coil inductance and the voltage drop across the coil.

14.3.2 Bridge-Tied Load (BTL)

Maximum output power:

$$P_{o(0.5\%)} = \frac{\left[\dfrac{R_L}{R_L + R_{DSon(hs)} + R_{DSon(ls)}} \times (V_{DD} - V_{SS}) \times (1 - t_{w(min)} \times 0.5f_{osc})\right]^2}{2R_L} \qquad (3)$$

Maximum output current internally limited to 12 A:

$$I_{o(peak)} = \frac{(V_{DD} - V_{SS}) \times (1 - t_{w(min)} \times 0.5f_{osc})}{R_L + (R_{DSon(hs)} + R_{DSon(ls)}) + 2R_{s(L)}} \qquad (4)$$

Where:

- $P_{o(0.5\ \%)}$: output power at the onset of clipping
- R_L: load impedance
- $R_{DSon(hs)}$: high-side R_{DSon} of power stage output DMOS (temperature dependent)
- $R_{DSon(ls)}$: low-side R_{DSon} of power stage output DMOS (temperature dependent)
- $R_{s(L)}$: series impedance of the filter coil
- $t_{w(min)}$: minimum pulse width (typical 150 ns, temperature dependent)
- f_{osc}: oscillator frequency

Remark: Note that $I_{o(peak)}$ should be less than 12 A; see Section 8.4.2. $I_{o(peak)}$ is the sum of the current through the load and the ripple current. The value of the ripple current is dependent on the coil inductance and the voltage drop across the coil.

14.4 External clock

To ensure duty cycle-independent operation, the external clock frequency is divided by two internally. The external clock frequency is therefore twice the internal clock frequency (typically 2 × 335 kHz = 670 kHz).

If several Class D amplifiers are used in a single application, it is recommended that all the devices run at the same switching frequency. This can be achieved by connecting the OSC pins together and feeding them from an external oscillator. When using an external oscillator, it is necessary to force pin OSC to a DC level above SGND. This disables the internal oscillator and causes the PWM to switch at half the external clock frequency.

The internal oscillator requires an external resistor R_{OSC}, connected between pin OSC and pin OSCREF. R_{OSC} must be removed when using an external oscillator.

The noise generated by the internal oscillator is supply voltage dependent. An external low-noise oscillator is recommended for low-noise applications running at high supply voltages.

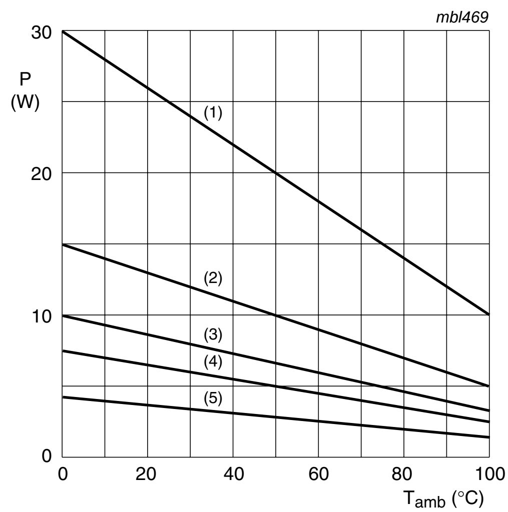
14.5 Heatsink requirements

An external heatsink must be connected to the TDA8954.

Equation 5 defines the relationship between maximum power dissipation before activation of TFB and total thermal resistance from junction to ambient.

$$R_{th(j-a)} = \frac{T_j - T_{amb}}{P} \quad (5)$$

Power dissipation (P) is determined by the efficiency of the TDA8954.



(1) $R_{th(j-a)}$ = 5 K/W.

(2) $R_{th(j-a)}$ = 10 K/W.

(3) $R_{th(j-a)}$ = 15 K/W.

(4) $R_{th(j-a)}$ = 20 K/W.

(5) $R_{th(j-a)}$ = 35 K/W.

Fig 12. Derating curves for power dissipation as a function of maximum ambient temperature

In the following example, a heatsink calculation is made for an 4 Ω SE application with a ±30 V supply:

The audio signal has a crest factor of 10 (the ratio between peak power and average power (20 dB); this means that the average output power is $\frac{1}{10}$ of the peak power.

Thus, the peak RMS output power level is the 0.5 % THD level, i.e. 92.5 W per channel.

The average power is then $\frac{1}{10} \times 92.5$ W = 9.25 W per channel.

The dissipated power at an output power of 9.25 W is approximately 9.5 W.

When the maximum expected ambient temperature is 50 °C, the total $R_{th(j-a)}$ becomes

$$\frac{(148 - 50)}{9.5} = 10.3 \text{ K/W}$$

$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)}$

$R_{th(j-c)}$ (thermal resistance from junction to case) = 0.9 K/W

$R_{th(c-h)}$ (thermal resistance from case to heatsink) = 0.5 K/W to 1 K/W (dependent on mounting)

So the thermal resistance between heatsink and ambient temperature is:

$R_{th(h-a)}$ (thermal resistance from heatsink to ambient) = 10.3 – (0.9 + 1) = 8.4 K/W

The derating curves for power dissipation (for several $R_{th(j-a)}$ values) are illustrated in Figure 12. A maximum junction temperature T_j = 150 °C is taken into account. The maximum allowable power dissipation for a given heatsink size can be derived, or the required heatsink size can be determined, at a required power dissipation level; see Figure 12.

14.6 Pumping effects

In a typical stereo single-ended configuration, the TDA8954 is supplied by a symmetrical supply voltage (e.g. V_{DD} = +41 V and V_{SS} = –41 V). When the amplifier is used in an SE configuration, a 'pumping effect' can occur. During one switching interval, energy is taken from one supply (e.g. V_{DD}), while a part of that energy is returned to the other supply line (e.g. V_{SS}) and vice versa. When the voltage supply source cannot sink energy, the voltage across the output capacitors of that voltage supply source increases and the supply voltage is pumped to higher levels. The voltage increase caused by the pumping effect depends on:

- Speaker impedance
- Supply voltage
- Audio signal frequency
- Value of supply line decoupling capacitors
- Source and sink currents of other channels

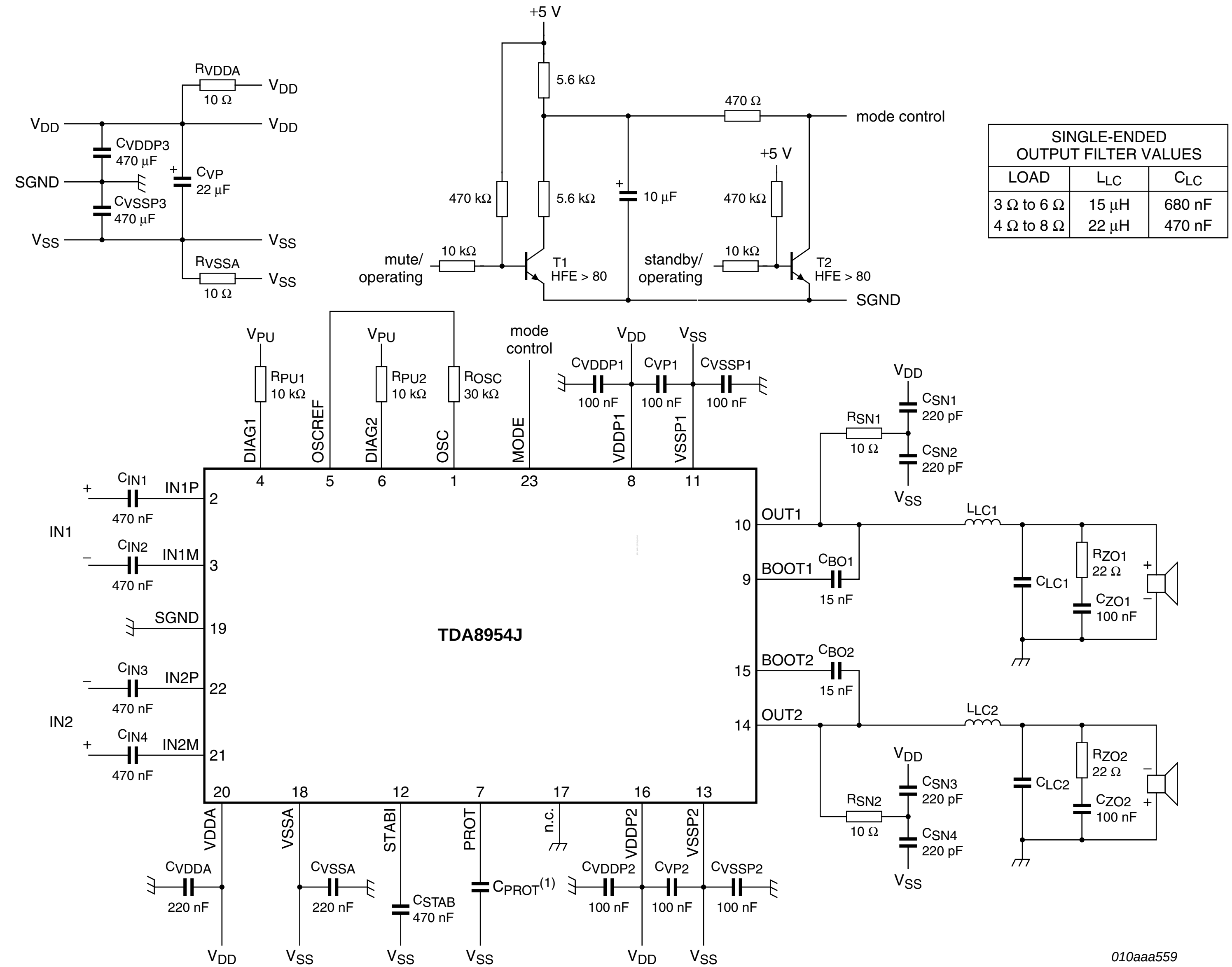
Pumping effects should be minimized to prevent the malfunctioning of the audio amplifier and/or the voltage supply source. Amplifier malfunction due to the pumping effect can trigger UVP, OVP or UBP.

The most effective way to avoid pumping effects is to connect the TDA8954 in a mono full-bridge configuration. In the case of stereo single-ended applications, it is advised to connect the inputs in anti-phase (see Section 8.5 on page 14). The power supply can also be adapted; for example, by increasing the values of the supply line decoupling capacitors.

14.7 Application schematic

Notes on the application schematic:

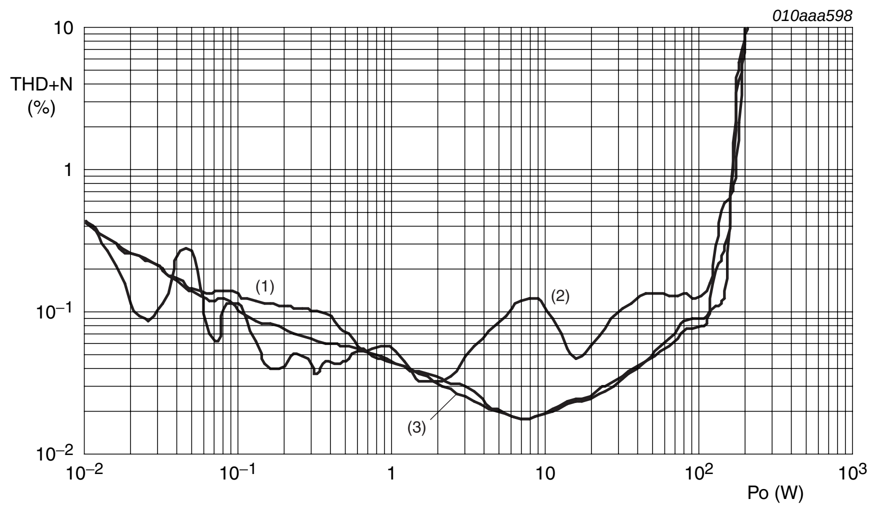
- Connect a solid ground plane around the switching amplifier to avoid emissions
- Place 100 nF capacitors as close as possible to the TDA8954 power supply pins
- Connect the heatsink to the ground plane or to VSSPn using a 100 nF capacitor
- Use a thermally conductive, electrically non-conductive, Sil-Pad between the TDA8954 heat spreader and the external heatsink
- The heat spreader of the TDA8954 is internally connected to VSSA
- Use differential inputs for the most effective system level audio performance with unbalanced signal sources. In case of hum due to floating inputs, connect the shielding or source ground to the amplifier ground.



(1) The value of C_{PROT} can be in the range 10 pF to 220 pF (see Section 8.4.2)

Fig 13. Typical application diagram

14.8 Curves measured in reference design (demo board TDA8954J)



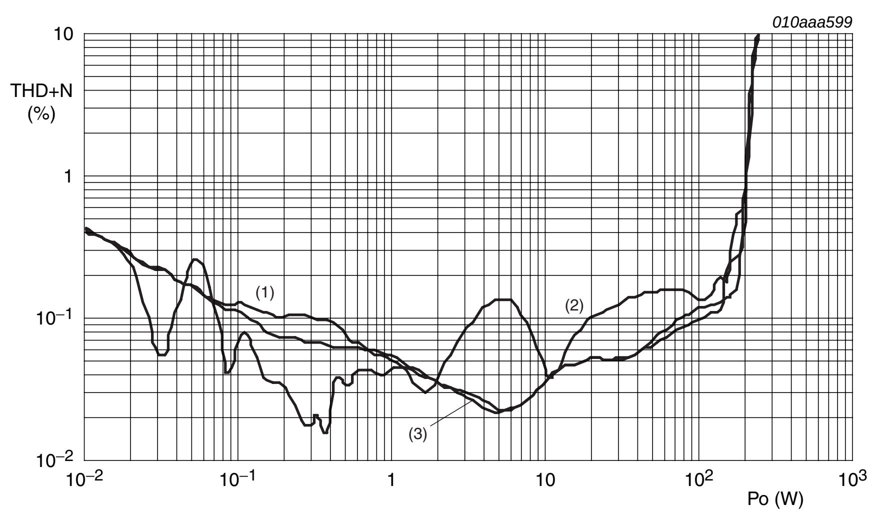
V_{DD} = 41 V, V_{SS} = −41 V, f_{osc} = 325 kHz (external 650 kHz oscillator), 2 × 4 Ω SE configuration.

(1) f_i = 1 kHz.

(2) f_i = 6 kHz.

(3) f_i = 100 Hz.

Fig 14. THD + N as a function of output power, SE configuration with 2 × 4 Ω load



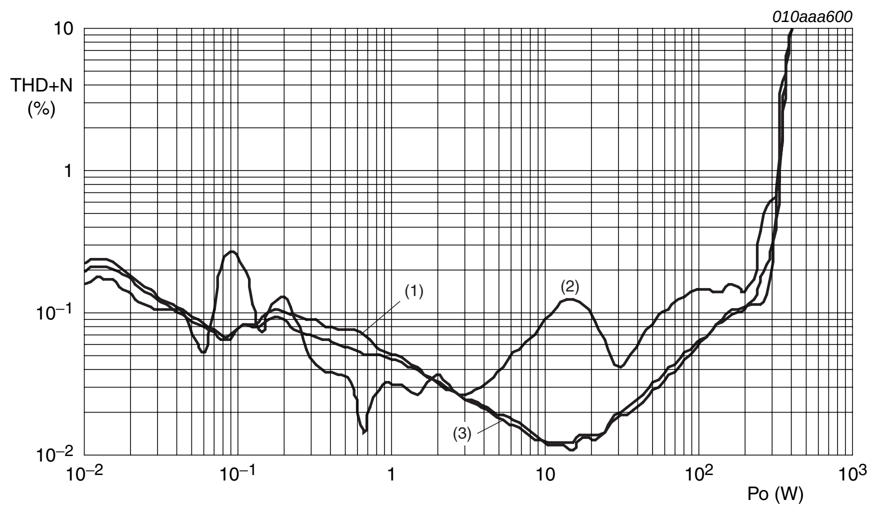
V_{DD} = 39 V, V_{SS} = −39, f_{osc} = 325 kHz (external 650 kHz oscillator), 2 × 3 Ω SE configuration.

(1) f_i = 1 kHz.

(2) f_i = 6 kHz.

(3) f_i = 100 Hz.

Fig 15. THD + N as a function of output power, SE configuration with 2 × 3 Ω load



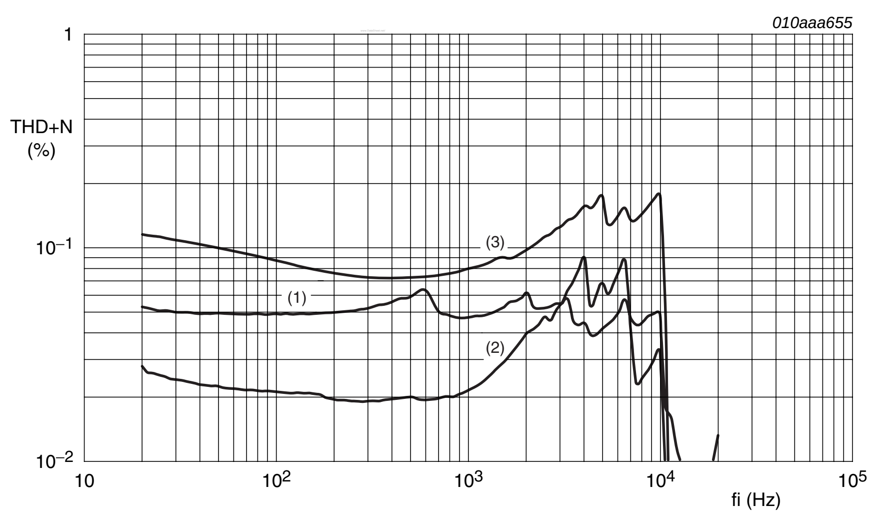
V_{DD} = 41 V, V_{SS} = −41, f_{osc} = 325 kHz (external 650 kHz oscillator), 1 × 8 Ω BTL configuration.

(1) f_i = 1 kHz.

(2) f_i = 6 kHz.

(3) f_i = 100 Hz.

Fig 16. THD + N as a function of output power, BTL configuration with 1 × 8 Ω load



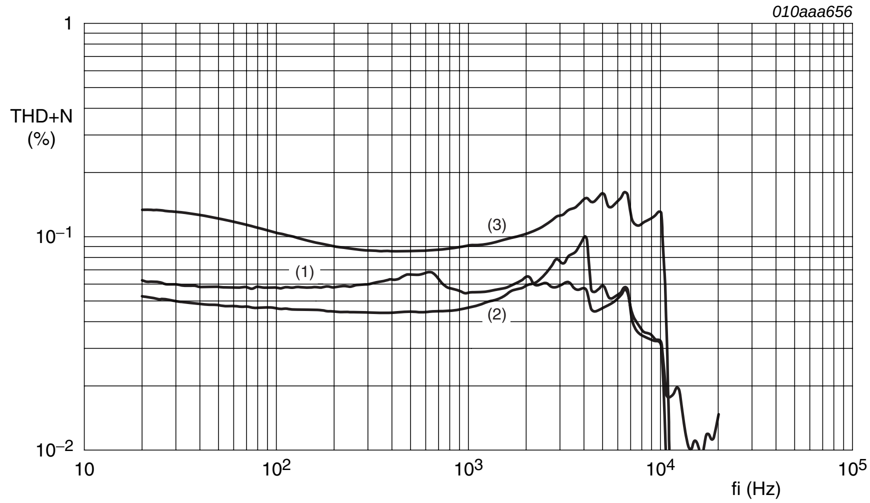
V_{DD} = 41 V, V_{SS} = −41, f_{osc} = 325 kHz (external 650 kHz oscillator), 2 × 4 Ω SE configuration.

(1) P_o = 1 W.

(2) P_o = 10 W.

(3) P_o = 100 W.

Fig 17. THD + N as a function of frequency, SE configuration with 2 × 4 Ω load



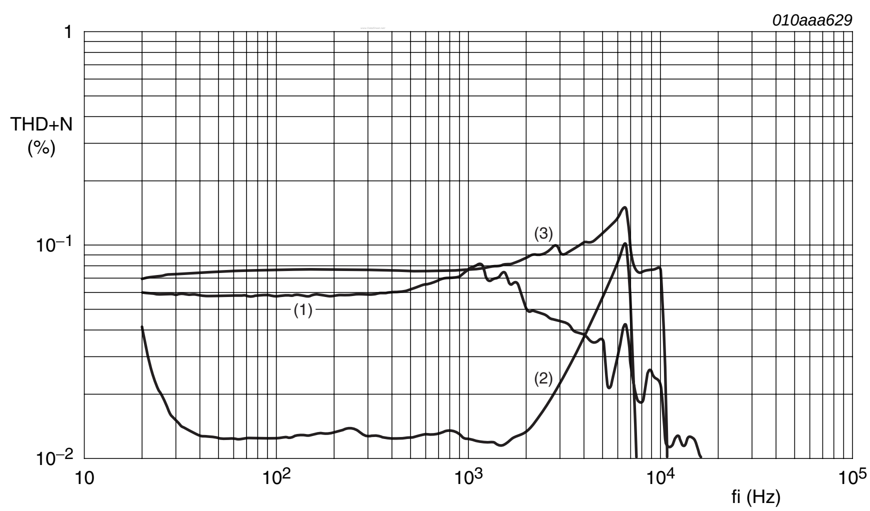
V_{DD} = 39 V, V_{SS} = –39, f_{osc} = 325 kHz (external 650 kHz oscillator), 2 × 3 Ω SE configuration.

(1) P_o = 1 W.

(2) P_o = 10 W.

(3) P_o = 100 W.

Fig 18. THD + N as a function of frequency, SE configuration with 2 × 3 Ω load



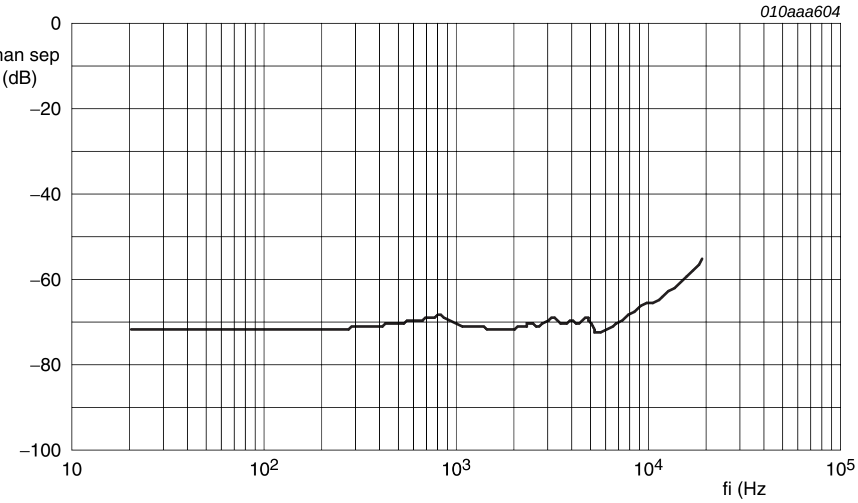
V_{DD} = 41 V, V_{SS} = –41, f_{osc} = 325 kHz (external 650 kHz oscillator), 1 × 8 Ω BTL configuration.

(1) P_o = 1 W.

(2) P_o = 10 W.

(3) P_o = 100 W.

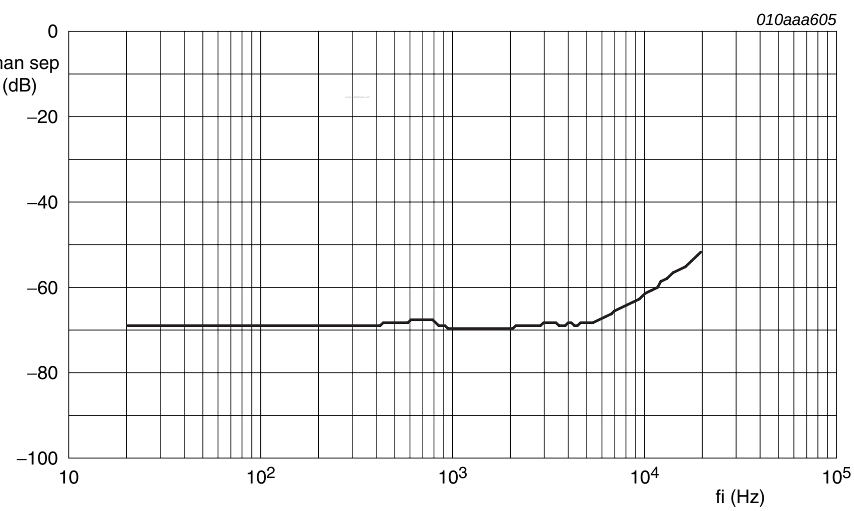
Fig 19. THD + N as a function of frequency, BTL configuration with 1 × 8 Ω load



V_{DD} = 41 V, V_{SS} = −41, f_{osc} = 325 kHz (external 650 kHz oscillator), 2 × 4 Ω SE configuration.

Channel B S/N (dB).

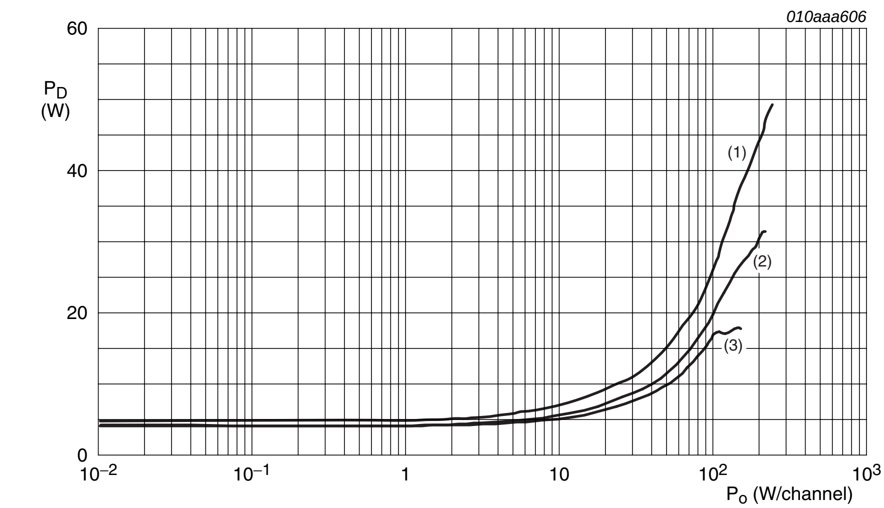
Fig 20. Channel separation as a function of frequency, SE configuration with 2 × 4 Ω load



V_{DD} = 39 V, V_{SS} = −39, f_{osc} = 325 kHz (external 650 kHz oscillator), 2 × 3 Ω SE configuration.

Channel B S/N (dB).

Fig 21. Channel separation as a function of frequency, SE configuration with 2 × 3 Ω load



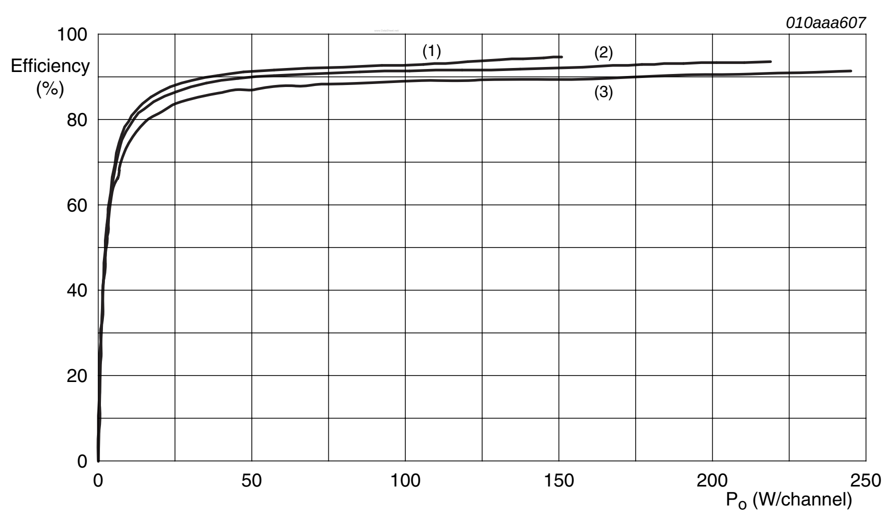
f_i = 1 kHz; f_{osc} = 325 kHz (external 650 kHz oscillator).

(1) 2 × 3 Ω SE configuration; V_{DD} = 39 V; V_{SS} = −39 V.

(2) 2 × 4 Ω SE configuration; V_{DD} = 41 V; V_{SS} = −41 V.

(3) 2 × 6 Ω SE configuration; V_{DD} = 41 V; V_{SS} = −41 V.

Fig 22. Power dissipation as a function of output power per channel, SE configuration



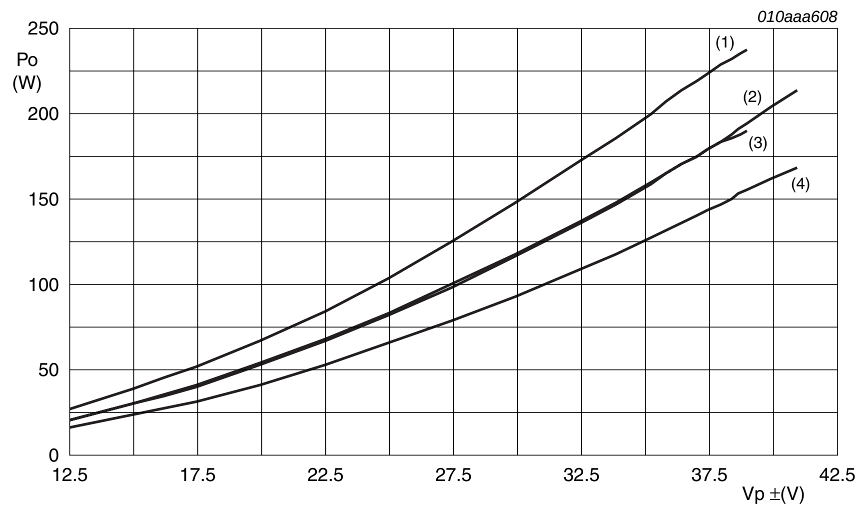
f_i = 1 kHz, f_{osc} = 325 kHz (external 650 kHz oscillator).

(1) 2 × 6 Ω SE configuration; V_{DD} = 41 V; V_{SS} = −41 V.

(2) 2 × 4 Ω SE configuration; V_{DD} = 41 V; V_{SS} = −41 V.

(3) 2 × 3 Ω SE configuration; V_{DD} = 39 V; V_{SS} = −39 V.

Fig 23. Efficiency as a function of output power per channel, SE configuration



Infinite heat sink used.

f_i = 1 kHz, f_{osc} = 325 kHz (external 650 kHz oscillator).

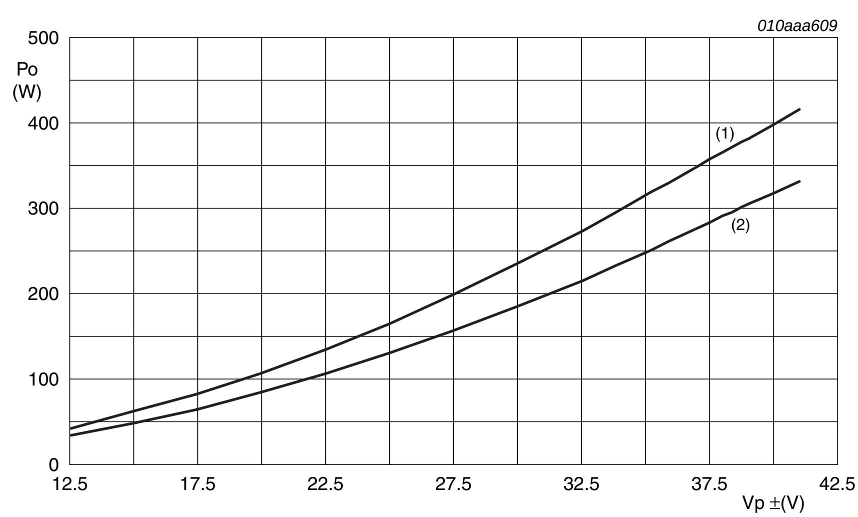
(1) THD + N = 10 %, 2 × 3 Ω.

(2) THD + N = 10 %, 2 × 4 Ω

(1) THD + N = 0.5 %, 2 × 3 Ω

(2) THD + N = 0.5 %, 2 × 4 Ω.

Fig 24. Output power as a function of supply voltage, SE configuration



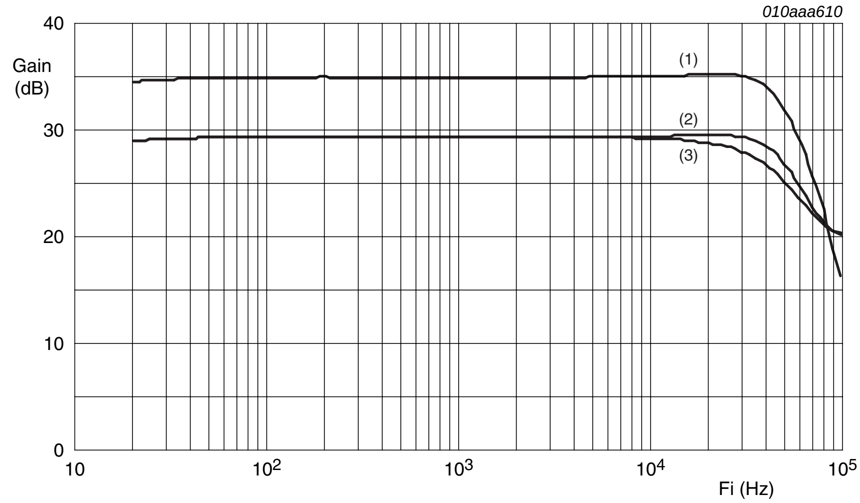
Infinite heat sink used.

f_i = 1 kHz, f_{osc} = 325 kHz (external 650 kHz oscillator).

(1) THD + N = 10 %, 8 Ω.

(2) THD + N = 0.5 %, 8 Ω.

Fig 25. Output power as a function of supply voltage, BTL configuration



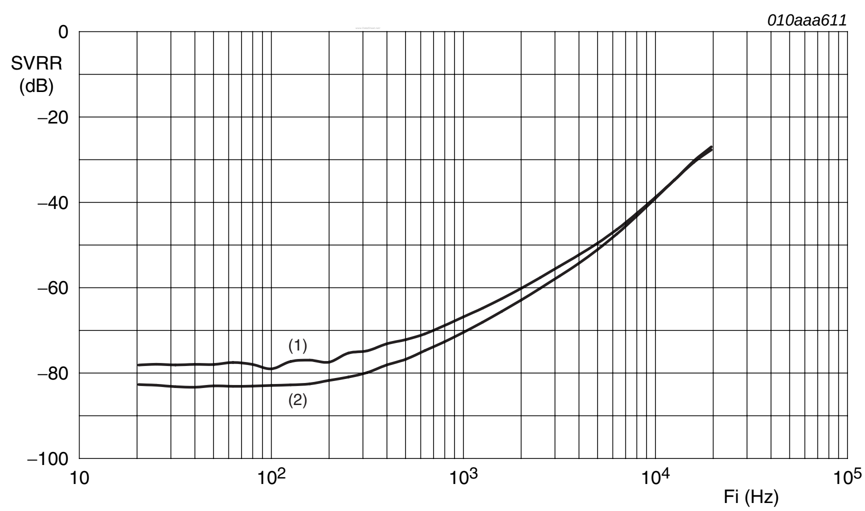
V_{DD} = 30 V, V_{SS} = –30 V, f_{osc} = 325 kHz (external 650 kHz oscillator), V_i = 100 mV, C_i = 330 pF.

(1) 1 × 8 Ω configuration; L_{LC} = 15 μH, C_{LC} = 680 nF, V_{DD} = 41 V, V_{SS} = –41 V.

(2) 2 × 4 Ω configuration; L_{LC} = 15 μH, C_{LC} = 680 nF, V_{DD} = 41 V, V_{SS} = –41 V.

(3) 2 × 3 Ω configuration; L_{LC} = 15 μH, C_{LC} = 680 nF, V_{DD} = 39 V; V_{SS} = –39 V.

Fig 26. Frequency response



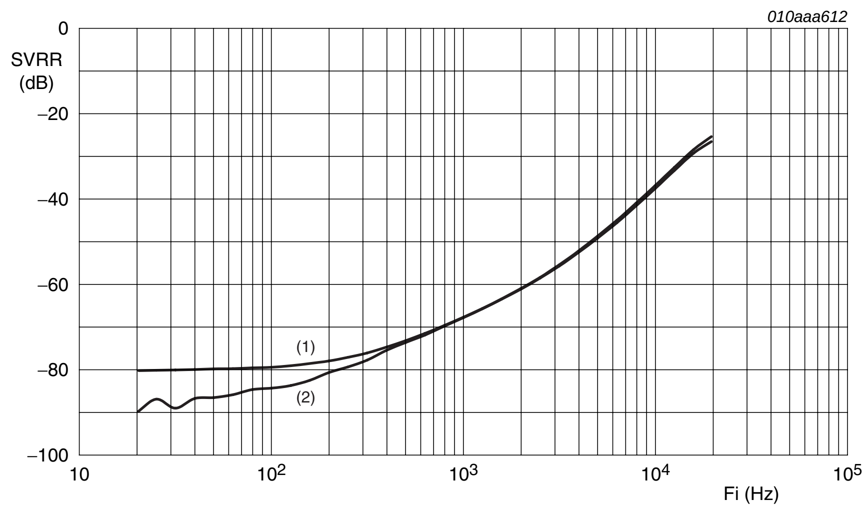
Ripple on VDD, short on input pins.

V_{DD} = 41 V, V_{SS} = –41 V, V_{ripple} = 2 V (p-p), 2 × 4 Ω SE configuration.

(1) Operating mode.

(2) Mute mode.

Fig 27. SVRR as a function of ripple frequency, ripple on V_{DD}



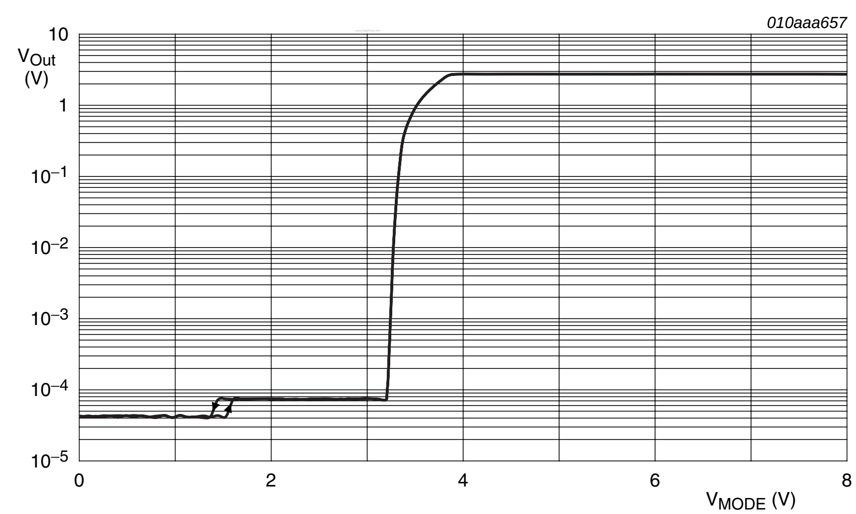
Ripple on VSS, short on input pins.

V_{DD} = 41 V, V_{SS} = −41 V, V_{ripple} = 2 V (p-p), 2 × 4 Ω SE configuration.

(1) Mute mode.

(2) Operating mode.

Fig 28. SVRR as a function of ripple frequency, ripple on V_{SS}

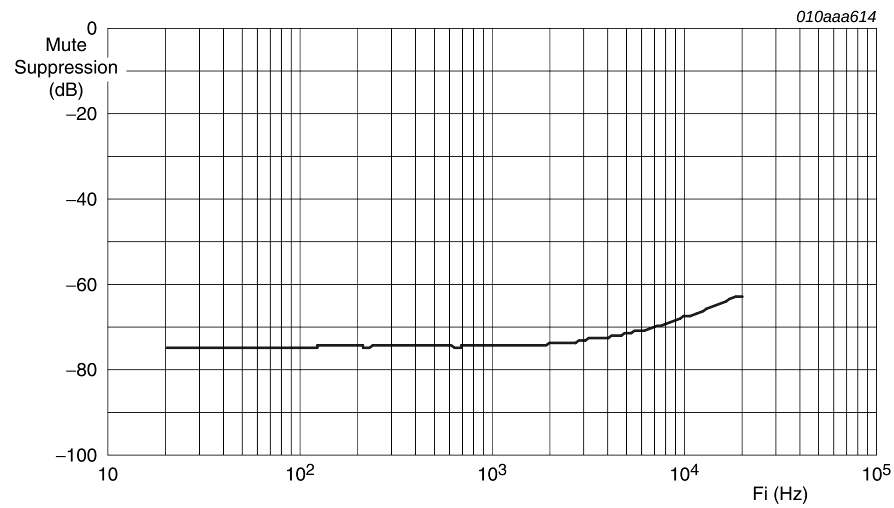


V_{DD} = 41 V, V_{SS} = −41 V, V_i = 100 mV, f_{osc} = 325 kHz (external 650 kHz oscillator), f_i = 1 kHz

(1) Mode voltage down.

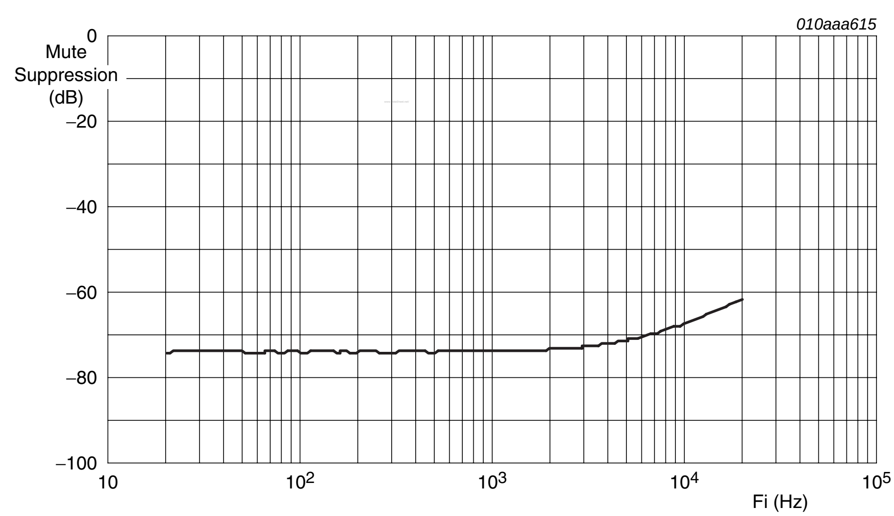
(2) Mode voltage up.

Fig 29. Output voltage as a function of mode voltage



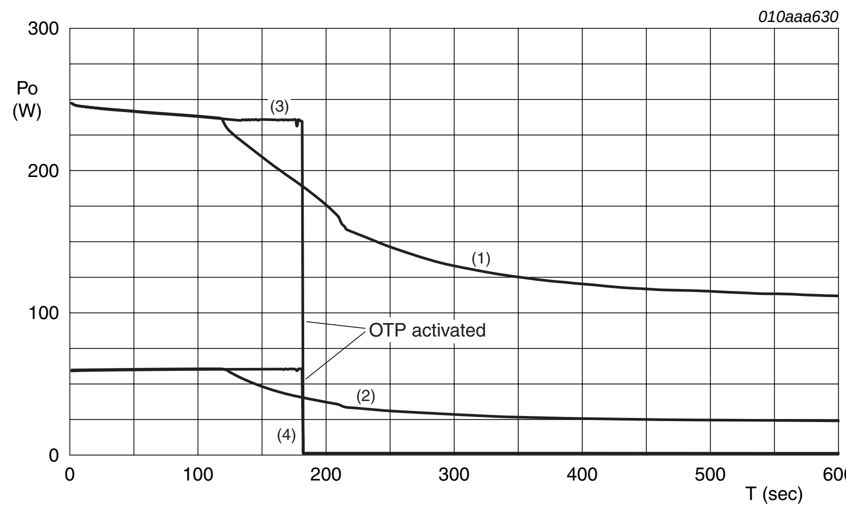
V_{DD} = 39 V, V_{SS} = −39 V, f_{osc} = 325 kHz (external 650 kHz oscillator), V_i = 2 V (RMS).
2 × 3 Ω SE configuration; channel A suppression (dB)

Fig 30. Mute attenuation as a function of frequency



V_{DD} = 41 V, V_{SS} = −41 V, f_{osc} = 325 kHz (external 650 kHz oscillator), V_i = 2 V (RMS).
2 × 4 Ω SE configuration; channel A suppression (dB)

Fig 31. Mute attenuation as a function of frequency



V_{DD} = 39 V, V_{SS} = –39 V, f_{osc} = 325 kHz (external 650 kHz oscillator), 2 × 3 Ω SE configuration.

Heat sink: Fisher SK495/50; Sil-Pad: 1500ST. Condition: 30 minutes pre-heated in Mute

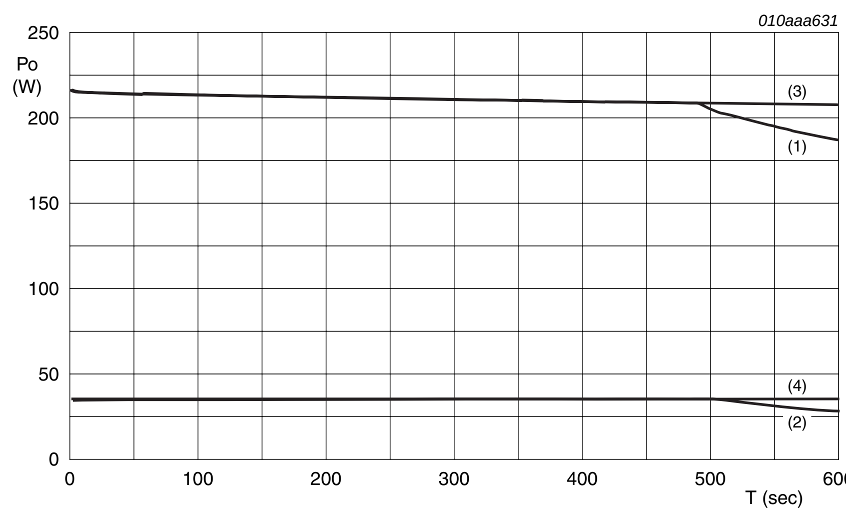
(1) Maximum output power; TFB on.

(2) Maximum output power / 8; TFB on.

(3) Maximum output power; TFB off.

(4) Maximum output power / 8; TFB off.

Fig 32. Output power as a function of time, 2 × 3 Ω



V_{DD} = 41 V, V_{SS} = –41 V, f_{osc} = 325 kHz (external 650 kHz oscillator), 2 × 4 Ω SE configuration

Heat sink: Fisher SK495/50; Sil-Pad: 1500ST. Condition: 30 minutes pre-heated in Mute

(1) Maximum output power; TFB on.

(2) Maximum output power / 8; TFB on.

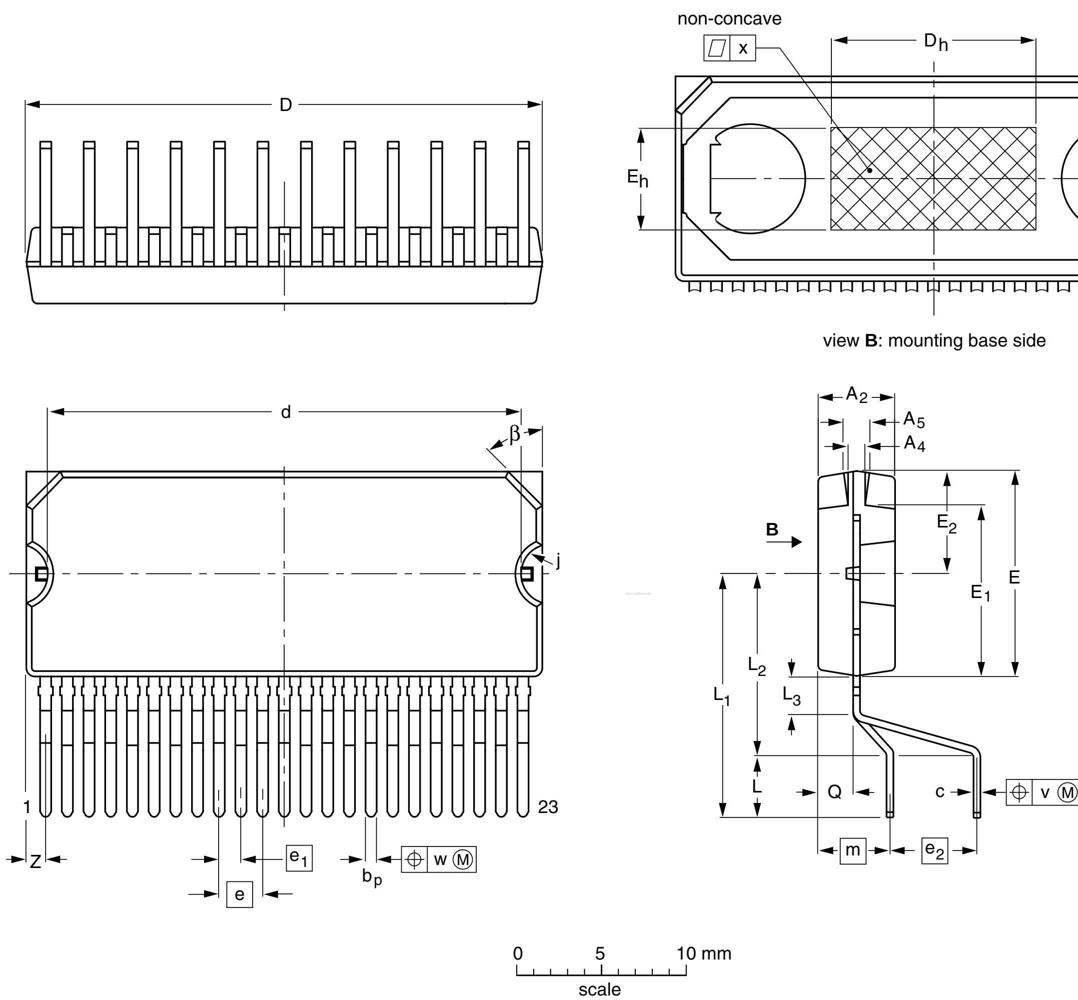
(3) Maximum output power; TFB off.

(4) Maximum output power / 8; TFB off.

Fig 33. Output power as a function of time, 2 × 4 Ω

15. Package outline

DBS23P: plastic DIL-bent-SIL power package; 23 leads (straight lead length 3.2 mm) **SOT411-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A_2	A_4	A_5	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	E_1	E_2	j	L	L_1	L_2	L_3	m	Q	v	w	x	β	$Z^{(1)}$
mm	4.6 4.3	1.15 0.85	1.65 1.35	0.75 0.60	0.55 0.35	30.4 29.9	28.0 27.5	12	12.2 11.8	2.54	1.27	5.08	6	10.15 9.85	6.2 5.8	1.85 1.65	3.6 2.8	14 13	10.7 9.9	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	45°	1.43 0.78

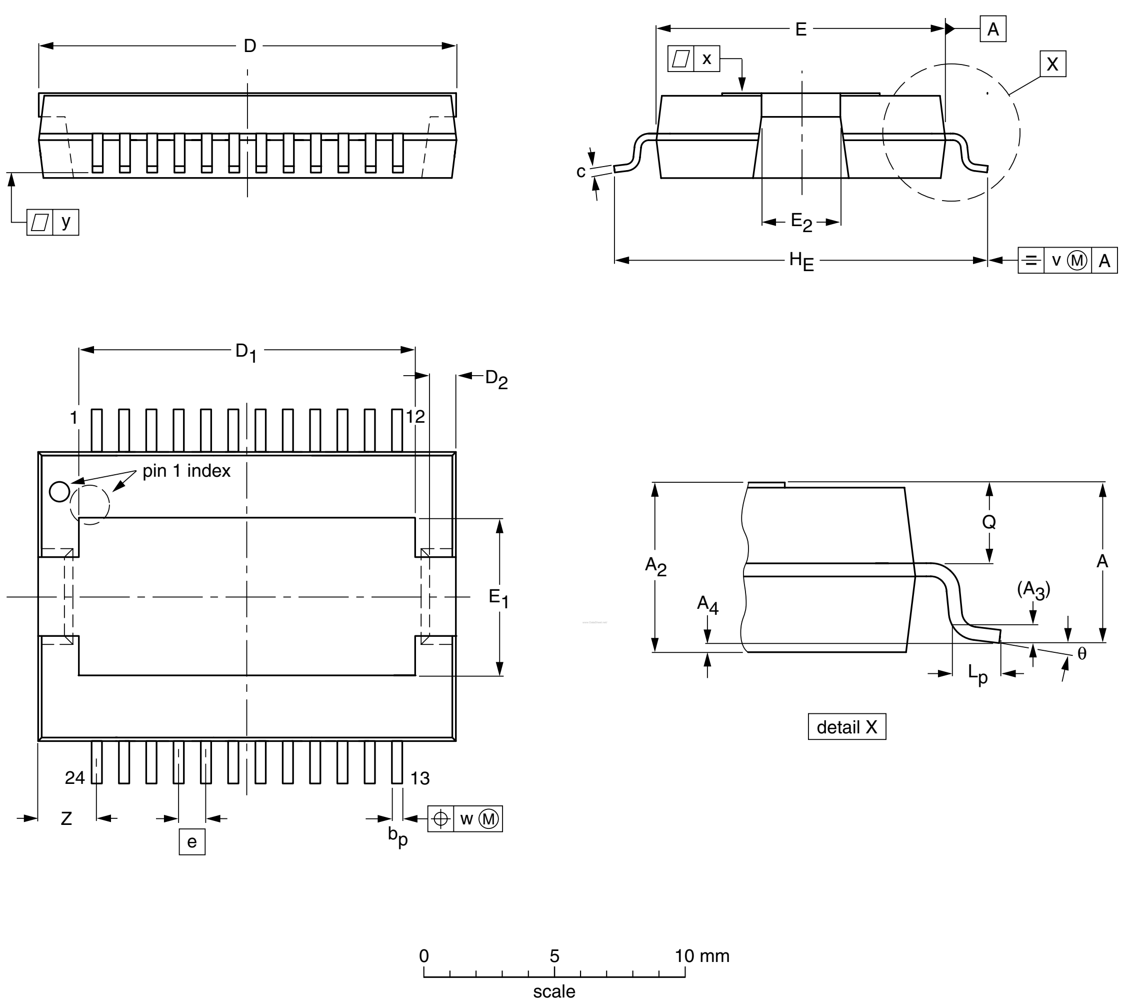
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT411-1						~~98-02-20~~ 02-04-24

Fig 34. Package outline SOT411-1 (DBS23P)

HSOP24: plastic, heatsink small outline package; 24 leads; low stand-off height **SOT566-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4(1)	b_p	c	D(2)	D_1	D_2	E(2)	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5	0.35	+0.08	0.53	0.32	16.0	13.0	1.1	11.1	6.2	2.9	1	14.5	1.1	1.7	0.25	0.25	0.03	0.07	2.7	8°
		3.2		−0.04	0.40	0.23	15.8	12.6	0.9	10.9	5.8	2.5		13.9	0.8	1.5					2.2	0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT566-3						~~03-02-18~~ 03-07-23

Fig 35. Package outline SOT566-3 (HSOP24)

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 36) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and 14

Table 13. SnPb eutectic process (from J-STD-020C)

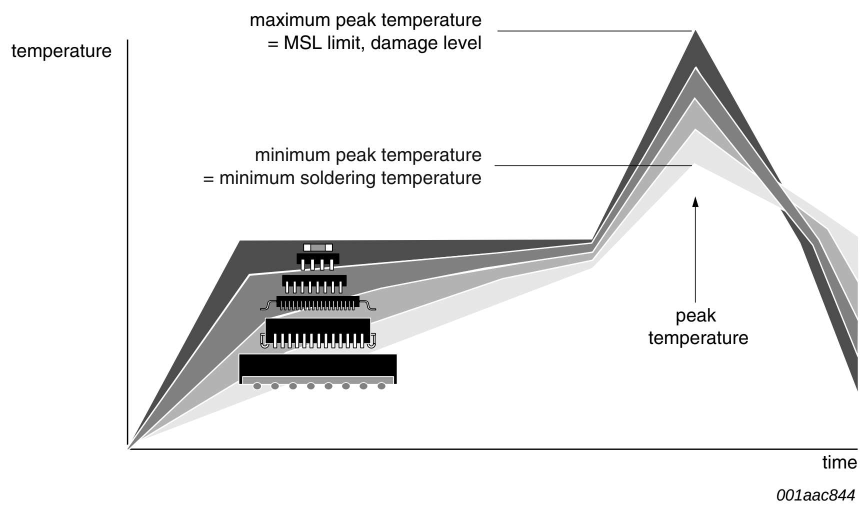
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 14. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 36.



MSL: Moisture Sensitivity Level

Fig 36. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

17. Soldering of through-hole mount packages

17.1 Introduction to soldering through-hole mount packages

This text gives a very brief insight into wave, dip and manual soldering.

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

17.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

17.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

17.4 Package related soldering information

Table 15. Suitability of through-hole mount IC packages for dipping and wave soldering

Package	Soldering method	
	Dipping	Wave
CPGA, HCPGA	-	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable[1]
PMFP[2]	-	not suitable

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

18. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8954_1	20091224	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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21. Contents

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